

## Research Article

# Development of Art and Culture Creative Industry Using FPGA and Dynamic Image Sampling

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The TVPS146's digital video processor is used for digital video processing and image output on digital signal processing (DSP) ports. The following is a summary of the field programmable gate array (FPGA) features and programming principles. FPGA is designed by the ping-pong operation, including serial to parallel conversion design, pipeline operation, and data interface synchronization. A dance video screenshot analysis microsystem is composed of it and video dynamic image processing. Finally, according to the number of dance culture performance institutions based on the internet from 2014 to 2018, the development strategy of dance culture and creativity based on the internet is put forward. The results show that the image sharpness of the video screenshots processed by the system is improved, and the effect of enhanced processing is achieved compared to the unprocessed video screenshots. In addition, after the video screenshot processed by the system is compressed, some details are lost and the outline of the image is blurred. The combination of internet immediacy, mass, grassroots, and interactivity can accelerate the development of China's dance culture and creative industry and provide an effective practical foundation for innovation in the development of art and culture.

## 1. Introduction

With the rapid development of China's economic level, people's demands for spiritual levels are increasing, and the manifestation of spiritual levels is undoubtedly the creative development of art and culture. Since China's Beijing Olympic Games shows the art stage with national characteristics to the world, electronic technology of different scientific and technological levels has been added to the stage design of the Spring Festival Gala every year, which perfectly combines sound effect and equipment [1, 2].

Since the conference on the reform of the cultural system, the state has demanded to improve the process of socialist cultural construction [3]. After the implementation of the spirit of the plenary session of the Central Committee, Chinese culture comes to a valuable golden period of development. In the east of the world, there is a cultural China with standardized market, scientific management, vigorous creation, and consumption [4]. Since then, various places in China have carried out the reconstruction of cultural facilities and the development of art and culture creative industries.

The development of dance art is an important part of it. All kinds of high and new technologies are applied to the construction of dance industry, thus promoting the rapid development of China's dance culture and creative industry [5, 6]. At the same time, the development of world cultural industry becomes intenser and intenser. As a part of dance art, drama develops rapidly in its industrialization process. The Broadway drama industry has developed into a core American art and culture creative industry that can keep pace with the Hollywood film industry and American record industry. The drama industry in the west end of London has made London the "capital of drama" and the cultural and creative center of the world [7–9]. The prosperity and development of the drama industry shows that dance art can form a creative industrialization road and lays the foundation for the creative development of Chinese dance industry.

When dancers constantly summarize their own road experience and carry out practical exploration on dance creative industrialization, it is particularly important to vigorously study the technology and equipment related to the creative development of Chinese dance industry [10]. Since

the 16th National Congress of the Communist Party of China decided to prosper the cultural industry, it has become a social consensus to develop the cultural industry creatively and rapidly. Dance is one of the oldest arts in human society. To make dance develop well in the world pattern of economic globalization, and continuously give play to its artistic creativity and charm, it is inevitable to take the road of industrialization [11, 12]. However, the late start of domestic cultural industry mode and the lack of outstanding talents and cutting-edge art and technology level hinder the development of domestic dance culture and creative industry.

Based on this, this exploration focuses on the research of cutting-edge technology in the dance culture and creative industry. Based on the field programmable gate array (FPGA) and dynamic image acquisition technology, a dance video image real-time processing system is proposed to analyze dance video in real time [13]. This system is flexible, convenient, and universal and belongs to the high-performance digital image acquisition and processing system. At the same time, constructive proposals for the future development of dance culture and creative industry are proposed based on the ideal height of establishing a high standard of the dance industry and the practical development of the dance culture and creative industry. It provides a theoretical basis for the development of the dance culture and creative industries, which have certain leadership and practical importance.

## 2. Method

*2.1. Dance Video Dynamic Image Processing Technology.* First, the input and acquisition of video dynamic image are performed. Analog processing and A/D conversion are used. In this exploration, Phase Alteration Line (PAL) video is used. After the switch selection of the input video is implemented, the signal is processed by simulation, automatic gain control, and A/D conversion. The resolution of the converted data is 10 bit, and the A/D conversion channel can receive the unified phase-locked loop (PLL) clock (in (25 MHz-30 MHz)). Figure 1 shows analog processing and A/D conversion. In factor analysis, the weight of each major factor is not determined and is determined by the percentage of the major factor that determines uterine change.

Then, digital video processing is performed. In this exploration, the digital video processor of TVPS146 is used. The processor can process many kinds of video formats and analyze the processing flow of the dance video processing circuit. In the video processing circuit, the output of A/D receives the digital dance video, performs Y/C separation, completes the chroma demodulation of the National Television Systems Committee (NTSC)/PAL, and enhances the luminance-bandwidth-chrominance (YUV) signal. The 10-bit dance video signal is multiplied by the subcarriers in the integral regulator to form a color difference signal. The  $U$  and  $V$  signals enter the low-pass filter to generate bandwidth that can be utilized [14]. Five adaptive comb filters [15] separate the  $U$  and  $V$  signals from  $Y$  and derive them. Then, the chroma and brightness are debugged to generate signal  $W$ . Furthermore, the output format of the chip can be 20-bit 4:2:2  $W$  or 10-bit 4:2:2  $W$ . Figure 2 shows the flow. With

certain performance improvements, there are new requirements for general adaptability and specific adaptability. The main problem with basketball gymnastics in Japan is that there are too many regular gymnastics, special gymnastics are not covered, and the obtained physical condition cannot be used for special gymnastics.

Human motion tracking based on template matching currently primarily uses error metrics between two matching pixel blocks. There are three main error metrics based on block matching: an error metric based on a cross-correlation function and a normalized mean square and finally, the image output. When the image is output through DSP port, the output interface of the video terminal is needed. The output interface consists of an online video display processor and a video encoder [16]. An online video display processor can display not only two different video windows and two different on-screen display (OSD) windows but also one video window, one OSD window, and one other attribute window. The frequency of video decoder in D/A conversion is 55 MHz, which can output video and audio in many formats such as NTSC/PAL. The output video signal can be directly transmitted to the monitor after D/A conversion to complete the output display. The maximum communication delay that the user can tolerate under the cloud and fog architecture is guaranteed, and the user's request is processed within the acceptable communication delay.

*2.2. Function Analysis of FPGA.* The maximum communication delay that the user can tolerate under the cloud and fog architecture is guaranteed, and the user's request is processed within the acceptable communication delay. FPGA is the core part of the system control and image processing and plays an important role. FPGA needs to carry out logic control, image preanalysis, image data storage control, and communication with DSP for image acquisition.

After the system is powered on, FPGA automatically loads the program through external electrically erasable programmable read-only memory (EEPROM). After receiving the instruction from DSP, FPGA starts to work, receives the imported image data signal, and separates the effective data according to its own working principle, to realize the control of image acquisition. The collected data are denoised, corrected, and enhanced, and the image data is converted to the YUV format. The processed data are exported to the external synchronous dynamic random access memory (SDRAM) through the SDRAM read-write control. SDRAM needs to be initialized before normal reading and writing. SDRAM can be initialized after being powered on for a period of time. The time required for this process cannot be determined, which is determined by the equipment used, usually 100  $\mu$ s; then, the Precharge command is transmitted to SDRAM. After Precharge is carried out in all pages, the SDRAM is refreshed. The purpose of refresh is to enable SDRAM to be configured normally. In this configuration, SDRAM can perform automatic Precharge, and the clock delay value depends on the dataset of SDRAM. The number of clock delays in this exploration is 3. The initialization process needs to comply with the parameters of the dataset of the

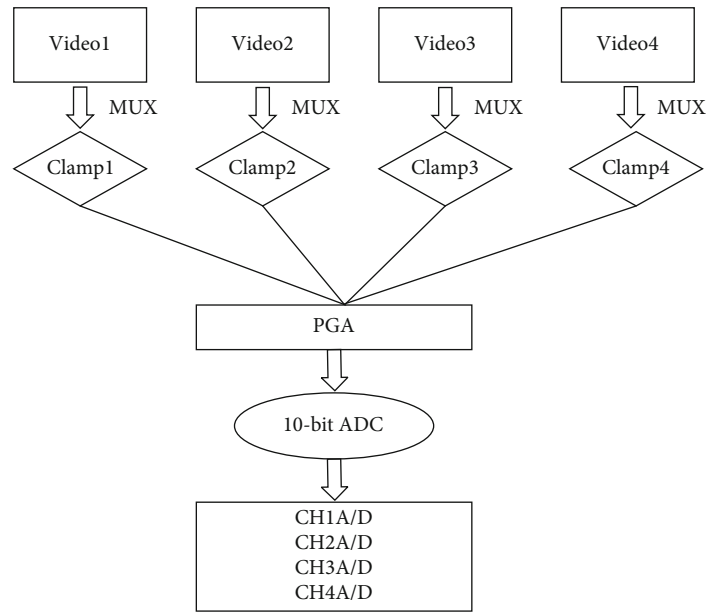


FIGURE 1: Video dynamic image simulation processing and A/D conversion.

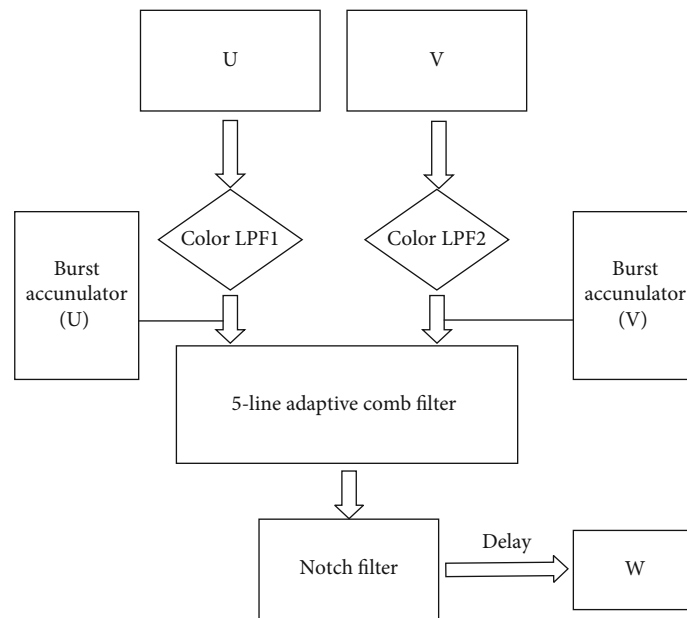


FIGURE 2: Digital video processing flow.

SDRAM chip. Otherwise, the normal initialization cannot be completed, which will directly make the subsequent SDRAM unable to read and write normally [17].

The decisive factors of SDRAM reading and writing content are DSP and image acquisition control module [18]. Its read-write control module mainly transmits the collected image data to SDRAM and reads the upper computer parameters written into SDRAM by DSP. To make the read-write speed reach the fastest level, SDRAM controller is equipped with two  $256 \times 2$  bit random access memory (RAM), both of which are in the FPGA. Its working speed is very fast. At the same time, the ping-pong operation is used to greatly improve the data transmission rate in FPGA. The law must be able to

effectively protect the interests of investors and creditors, to contribute to the establishment and maintenance of good economic order, and thus to ensure the smooth and efficient operation of the financial system. A well-developed credit system can not only effectively reduce the cost of information collection but also reduces the negative choice and moral hazard caused by information asymmetry and reduces the occurrence of financial gaps and financial crises.

*2.3. FPGA Programming Principles.* In this study, the principle of designing a system is that the system belongs to a hardware system. However, the FPGA design must consider how a single board completes module task assignments, the type of

algorithm suitable for use with the FPGA, and the capabilities it provides. This indicates that the system must have the proper placement of global macros such as clock domain and execution speed.

In general, the functional modules with high real-time requirement and high frequency can be realized by the FPGA/-complex programmable logic device (CPLD). Compared with CPLD, FPGA is more suitable for the design of wide scale, high frequency, and large number of registers. Compared with PLD's rich combinational logic, FPGA's triggers are very rich. In terms of FPGA design ideas, the use of four common design ideas can maximize the use efficiency [19].

### (1) Ping-pong operation

The ping-pong operation can be often applied to data stream control and processing. Figure 3 shows the classic ping-pong operation mode [20].

The ping-pong operation processing steps are as follows.

First, input the data stream. The input data selection module divides the data stream into two different data buffer areas. The data buffer area can hold any storage module and commonly used storage unit such as dual-port RAM, single-port RAM, and first input first output (FIFO).

Second, in the first buffer cycle, the imported data stream is cached to the first data buffer module. In the second buffer cycle, the input data selection unit is switched to cache the input data stream to the second data buffer module. At the same time, the data of the first cycle cached by the first data buffer module is transferred to the data stream operation and processing module after specific selection.

Third, in the third buffer cycle, the imported data stream is cached to the first data buffer module by switching the data again, and the cache data of the second data buffer module is switched through the "input data selection unit" to reach the "data stream operation processing module" to complete the operation and processing. From the first step to the third step, the cycle is carried out.

The core feature of the ping-pong operation is to switch through "input data selection unit" and "output data selection unit" according to a certain rhythm and send the buffered data stream to the "data stream operation processing module" at a stable speed to complete the operation and processing. The ping-pong operation module belongs to a whole, and the module's input data stream and output data stream will not produce any pause, so it is very suitable for pipeline processing of data stream. Therefore, the ping-pong operation is usually applied to the pipeline algorithm to realize seamless buffering and processing of data. Another characteristic of the ping-pong operation is that it can save buffer interval. Using the ping-pong operation, only two RAM which can buffer one time slot data need to be defined. If data are read from another RAM while data is written to one RAM and sent to the processing unit for processing, the capacity of each RAM is only 256 bits.

### (2) Design of series to parallel conversion

Serial to parallel conversion is an important skill in the FPGA design, a common way of data stream processing,

and a direct embodiment of the idea of area and speed exchange. There are many ways to realize serial to parallel conversion. The selected registers and RAM can complete the sorting and quantity requirements according to the data. In the ping-pong operation diagram, DPRAM is used to complete the serial to parallel conversion of the data stream. Because of the use of DPRAM, the data buffer area can be opened very large. For a small number of designs, the register can be used to complete the serial to parallel conversion. If there is no special requirement, a synchronous timing design can be used for the conversion between serial and parallel.

### (3) Pipeline operation

The pipeline proposed in this exploration refers to a design idea of processing flow and sequential operation [21], which is not the design idea used to optimize timing in application-specific integrated circuit (ASIC) design. Pipeline processing is a common design method in high-speed design. If the processing flow of a design is divided into several steps, and the whole data processing is "single flow," there is no feedback and iterative operation. Moreover, the output of the previous step is the import of the next step, so it is necessary to consider using the pipeline design method to improve the working frequency of the system. Its basic structure is as follows. All the operation steps divided properly are connected in a single flow direction. The biggest characteristic and requirement of pipeline operation is that the processing of data stream in each step is continuous in time. If each operation step is simplified and assumed to start with a trigger, the pipeline operation can be regarded as a shift register group, and the data stream flows through the trigger in sequence. Finally, the work of each step is completed. The key point of the pipeline design is the proper arrangement of the whole design sequence and the reasonable division of each operation step [22, 23].

### (4) Data interface synchronization

First, if the beat of the input data and the processing clock of the current chip have the same frequency, the master clock of the current chip can be used to complete the register sampling and the synchronization of the input data. Second, if the input data is not synchronized with the processing clock of the current chip, especially when the frequency does not match, the synchronization of the input data can be realized only by using the processing clock to carry out register sampling for the input data twice. The register is used to sample the data in the asynchronous clock domain twice, which can effectively prevent the unstable propagation of the data state and make the data processed by the later stage circuit effective. However, this method cannot guarantee that the data sampled by two-stage registers is correct, and there will be a certain amount of wrong data. Therefore, it is only applicable to functional units that are not sensitive to a small number of errors [24, 25]. In order to avoid wrong sampling in the asynchronous clock domain, RAM and FIFO are usually used to realize data conversion in the asynchronous clock domain. The buffer unit used most is DPRAM. In the input port, the upper clock is used to write data, and the current level clock

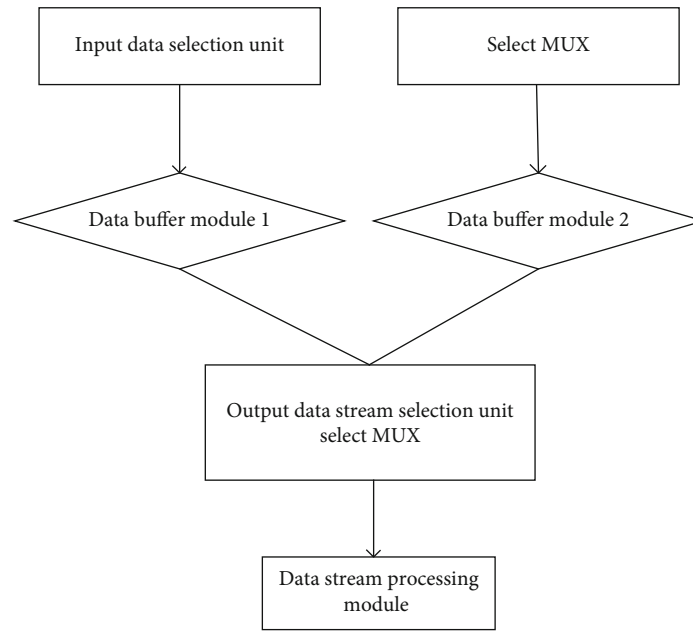


FIGURE 3: Ping-pong operation steps.

is used to read data at the output port. Thus, it is very convenient to implement the data exchange between asynchronous clock domains.

Finally, data exchange is carried out. The video data transmission methods between FIFO and DSP in FPGA are usually software query, interrupt data, and enhanced direct memory access (EDMA). Software query consumes too much central processing unit (CPU) resources, while interrupt data transmission can save a lot of CPU time, but it cannot play an appropriate EDMA resource. The development foundation of EDMA is direct memory access (DMA), which can convert data between different storage spaces without CPU. DM6437 in this exploration can provide 64 independent EDMA channels. The priority of the channel can be programmed. Without the participation of CPU, high-speed data transfer between on-chip memory, on-chip peripherals, and external storage space is realized. Therefore, in order to reduce the burden of CPU and exert the powerful external data transmission ability of DM6437, the video image acquisition unit sends out a EDMA transmission request and establishes an EDMA channel to complete the transmission of video data from FIFO to LZSRAM and SDRAM.

### 3. Results and Discussion

**3.1. System Image Analysis Results.** The system proposed in this exploration captures the image of dance video. After debugging, the outputs are shown in Figures 4–6.

Figure 4 is the original video screenshot without any processing, Figure 5 is the image processed by the system, and Figure 6 is the image after 10 times compression after the system processing. Compared with Figure 4, the sharpness of the image in Figure 5 is improved, and the effect of the enhancement process is obtained. Compared to Figures 4

and 5, some details are lost in Figure 6 and the outline of the image is quite blurry.

Image compression will cause loss to the file, so some details will be lost. According to the results of image output, the system proposed in this exploration can achieve the optimization of video image and achieve the ideal level.

**3.2. The Number of Dance Culture and Creative Performance Institutions Based on Internet.** According to the data of the State Statistical Bureau, the number of internet-based dance culture and creative performance institutions is shown in Figure 7.

Figure 7 shows that from 2014 to 2018, the number of state-owned and collective dance performance institutions remains at a certain number, basically unchanged, while the dance performance institutions based on the internet show a growing trend. Especially after 2016, the growth rate increases significantly. The internet is characterized by immediacy, massiveness, grassroots, and interactivity. The dissemination of dance content and dance resources on the internet platform not only enhances the vitality of dance art but also provides materials for dance content producers, which helps to stimulate the creative inspiration and creative power of producers.

For consumers of dance products, the internet platform provides them with convenient channels for retrieval, comparison, selection, payment, and sharing. In terms of retrieval, comparison, and selection, the network platform enables them to quickly obtain all-round dance product information and lock in the required products according to their own needs; the payment function saves time and cost for consumers' purchase and payment, and it is more convenient to obtain dance products or dance experience at the most favorable price through "shop around." By sharing an internet platform, consumers often gather in specific



FIGURE 4: Original video screenshot.



FIGURE 5: Video screenshot after system processing.



FIGURE 6: Compressed image.

communities or sites for communication. This is also the spread of dance products. For dance product promoters, the internet platform is a cheap, convenient, and efficient promotion platform. Compared to manual promotions, internet platforms help eliminate complex intermediate links, save costs, and accelerate promotions. It is also an

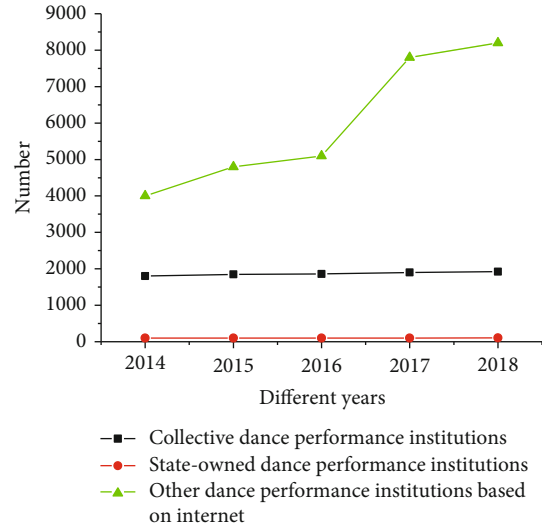


FIGURE 7: Number of dance performance institutions.

internet-based development strategy for dance culture and creativity [26].

#### 4. Conclusion

This study uses the main processor DM6437, which is suitable for single-channel video processing systems, as the main chip. First, stage video dynamic image processing is performed. Then, use the ping-pong operation to design the FPGA. This includes serial to parallel conversion design, pipeline operations, and data interface synchronization. You can complete fast external data exchange and data manipulation. The proposed architecture is flexible and has strong generality. It can be modularized to improve the efficiency of the algorithm. In addition, the short development cycle makes it convenient for system maintenance and upgrades. The system can capture and process dynamic images of video. The sharpness of the obtained image is improved, the image quality is greatly improved, and the internet can be widely used.

At the same time, according to the increasing number of dance culture performance institutions based on the internet from 2014 to 2018, the development strategy of dance culture and creativity is put forward. The dance content and dance resources are spread on the internet platform, providing consumers with convenient retrieval, comparison, selection, payment, and sharing channels, so that they can gather in a certain community or site for communication, and quickly obtain all-round dance product information, and lock in the required products according to their own needs. Consumers can get dance products or dance experience at the most favorable price. Moreover, the internet platform provides a low-cost, convenient, and efficient promotion platform for promoters. It not only enhances the vitality of dance art but also provides materials for dance content producers, which helps to stimulate the creative inspiration and creative power of producers. Compared with manual promotion, the internet platform eliminates the complex intermediate links, saves the cost, and thus speeds up the

promotion speed. Due to personal and time reasons, there are still some deficiencies in this exploration. The dynamic acquisition speed and image output quality of the dance video are not well controlled, which is the focus of the follow-up study and needs to be further improved.

## Data Availability

No data were used to support this study.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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