Hindawi
Wireless Communications and Mobile Computing
Volume 2022, Article ID 3016709, 10 pages
https://doi.org/10.1155/2022/3016709

Research Article

An Improved Harmony Search Approach for Block Placement for VLSI Design Automation

Shaik Karimullah,[1] **D. Vishnuvardhan**,[1] **Muhammad Arif**,[2] **Vinit Kumar Gunjan**,[3] **Fahimuddin Shaik**,[4] **and Kazy Noor-e-alam Siddiquee**[5]

[1]*Department of Electronics and Communication Engineering, JNTUA Ananthapuramu, Andhra Pradesh, India*
[2]*Department of Computer Science and Information Technology, University of Lahore, Pakistan*
[3]*Department of Computer Science and Engineering, CMR Institute of Technology Hyderabad, India*
[4]*Department of Electronics and Communication Engineering, Annamacharya Institute of Technology & Sciences, Rajampet, India*
[5]*Department of Computer Science and Engineering, University of Science and Technology, Chittagong, Bangladesh*

Correspondence should be addressed to Kazy Noor-e-alam Siddiquee; knas11@gmail.com

Received 1 March 2022; Revised 30 March 2022; Accepted 7 April 2022; Published 29 April 2022

Academic Editor: Nawab Muhammad Faseeh Qureshi

The technology grows quickly in the area of the VLSI physical design; it is crucial to integrate the greater number of transistors and parts into a very small range. Before the placement is completed, the physical and technical positioning of the blocks in the chip area is planned, which is nothing but floor planning. In order to lessen the placement region in the physical layout, floor planning must be carried out effectively. This paper proposes a blended harmony search and particle swarm optimization (BHSPS) algorithm which is the deliberate blend of the harmony search (HS) algorithm, and the particle swarm optimization (PSO) algorithm is proposed to acquire the central goal of the VLSI placement strategy. The objective here is to lessen the field of plan. The MATLAB code for the blended harmony search and particle swarm optimization (BHSPS) algorithm is compiled, and investigations were carried out for better examination through the standard MCNC, i.e., North Carolina Microelectronics Center benchmark circuits.

1. Introduction

As the demand for the new technology is growing on the market, the IC design sector has conducted more study, which in turn makes the VLSI design established with more composite, more reliable, more compact, and better results. The IC architectural design has been much more complex as there are countless numbers of transistors in one chip. For hierarchical, building block design methodology, floor planning is a more complicated approach to the abovementioned problem, which is an important design phase. As the size of the circuit increases, the space of the solution also increases, rendering the global solution hard to understand [1]. After partitioning, in the next step, called floor planning, the complex circuit is split into smaller circuits.

The BHSPS algorithm is used to optimize the chip area and routing wirelength during the placement of macroblocks. The IHS algorithm was developed by integrating the best characteristics of the harmony search algorithm and the nature-inspired particle swarm optimization algorithm. The integration of the harmony search (HS) and particle swarm optimization (PSO) algorithms yields the BHSPS algorithm. The hybridization is accomplished by the use of a forward-cascading approach between the harmony search (HS) algorithm and the particle swarm optimization (PSO) algorithm. Because of their separate greatest performances, HS and PSO have been combined. HS is a highly fast algorithm that provides results quickly, but PSO has a sluggish convergence rate but can produce virtually superior answers. The Improved harmony search (IHS) algorithm is presented

for the purpose of floor planning in VLSI physical design automation to obtain required performance while maintaining both speed and accuracy.

In order to condense the total unused area in the plan of a circuit and to minimize the total space of the chip used by the circuit, it is used to calculate the relative positions of the various modules in each subcircuit. A variety of stages in the physical design of ICs are partitioning, floor planning, positioning, routing, and compaction. In the manufacture of ICs, the VLSI design process is an important factor.

Placement is a crucial step in the automation of the electronic design, part of the physical design flow that assigns accurate locations within the chip main area for various circuit components [2, 3]. A lower positioning job can also make it unproduced by producing an excessive wire length beyond available routing resources in relation to influencing the effectiveness of the chip. Thus, a placer must perform the task in order for a system to satisfy its performance requirements by optimizing a number of goals. Optimization is a fully complete, functional, or efficient action, process, or methodology to make something (as design, system, or decision), specifically mathematical procedures (as a function maximum) engaged here [4, 5]. It is an area of applied mathematics whose principles and techniques are applied in fields including physics, biology, engineering, and economics to resolve quantitative issues. The same mathematical instruments can be used to resolve questions concerning maximizing or minimizing features in multiple fields.

Harmonic search is a music improvement metaheuristic algorithm [6]. The conviction that music is looking for an ideal state motivated the perception. This agreement in music is closely resembling optimality in an enhancement cycle. The journey technique for enhancement can be contrasted with a jazz performer's unplanned creation process [7–9]. From one viewpoint, the ideal agreement is indicated by the standard of sound style. A performer consistently needs to make a totally agreeable bit of music. Both procedures are designed to deliver the good or best. Such similarities between two procedures can be used by learning from one another for the development of fresh algorithms [10, 11]. Harmony search's best example is to transform the qualitative improvisation into some quantitative laws by the invention and thus the loveliness and coherence of music into a method of optimization by finding a perfect harmony, namely, a harmony search [12, 13].

2. Related Work

As VLSI advances have grown, new plan patterns have showed up. Due to component size and sign defer cutback, throughout 80% of the total chip area, all-out time postpone now compares to interconnection delays. In this specific circumstance, the arrangement is becoming progressively significant and new strategies are required [14]. The fundamental bit of the scope of transformative strategies is that they give a bunch of elective answers for equal registering. They are an amazing asset for beating nearby optima [15]. One answer for the VLSI position is particle swarm optimization [16]. This methodology is exceptionally viable at the underlying situation stage.

In [17], the authors projected a developmental calculation known as craziness-based PSO for streamlining the floor arranging of a VLSI chip. It was utilized to accelerate nearby inquiries and improve the exactness of the arrangement. The fundamental goal of floor arranging advancement is to limit the chip zone and the total wirelength. In [18], authors zeroed in on the multitarget bat calculation (MOBA), a naturally roused metaheuristic spasm, and effectively utilized it to recover the floor arranging in the VLSI plan. The calculation's key thought is to mimic bats' echolocation capacities to advance the situation. The spot meant was considered as a multiobjective optimization (MOO) issue, wherein equivalent significance was given to wirelength reduction and deduction of dead space.

To progress the nature of a VLSI execution, [19] proposed another temp-vulnerability detailing during the clock-tree amalgamation measure called stochastic perturbation-based clock streamlining (SPECO). The examination considers the impact of a chip's temperature deviation on the synchronization quality, which thus affects the speed of present-day VLSI chips. Exploratory outcomes demonstrated a critical decrease in the dephasing and computational convolution. To improve the nature of a VLSI usage, Basir-Kazeruni proposed another temperature-vulnerability plan during the clock-tree combination measure called stochastic annoyance-based clock enhancement (SPECO). The examination considers the impact of a chip's temperature variation on the synchronization quality, which thus affects the speed of the current VLSI chips. Exploratory outcomes indicated a critical decrease in the dephasing and computational multifaceted nature.

The outcomes indicated that the new algorithm stayed away from the low combination rate in the underlying phase of an essential subterranean insect province framework. The proficiency of the forbidden subterranean insect province framework improved by around 16.667%, compared to accessible methodologies. In addition, it adequately dodged nearby optima. The proposed calculation included consolidating a populace search-based improvement approach, explicitly, PSO, and a nearby inquiry-based strategy. Albeit and his fellow researchers have attempted for the improvement of the VLSI situation by developing new calculations and procedures; the high-computational algorithms complicated the natural issue and have not been addressed for a solution. In [19], researchers zeroed in on the idea of MOO while mechanizing the arrangement in a simple coordinated circuit format plan. An inventive file-based multiobjective mimicked tempering calculation, working over an outright portrayal, is proposed to upgrade the position of every nearness gathering. Rather than conventional single-target arrangement draws near, the subsequent Pareto fronts compromises between the streamlining destinations of each gathering, are consolidated, through the plan progressive system, until a last front is achieved. Thus, the unpredictability is decreased and split over different executions of the enhancement portion with less plan factors is attained.

It has been introduced in a work called PASSIOT [18], another approach for multiobjective and improved synthesis

of simple circuits, in light of figuring Sobol's lists for the vectors of their variable boundaries. PASSIOT was reenacted utilizing genuine streamlining capacities and was demonstrated serious regarding runtime and arrangement quality. In [18], to improve productivity in a multiobjective thermally mindful nonslicing floor arranging strategy, a versatile hybrid-memetic calculation was introduced to upgrade the zone, complete wirelength, and most extreme and normal temperatures of a chip. In the proposed calculation in [19], a hereditary inquiry calculation is utilized as a worldwide hunt strategy to investigate the pursuit space however much as could be expected. An adjusted reproduced strengthening search calculation is utilized as a nearby hunt strategy to misuse the data in the inquiry. The worldwide investigation and neighborhood manipulation are adjusted by a passing likelihood system. Trial results on standard test benchmarks demonstrated that the proposed calculation effectively got floor plans, while diminishing the normal and highpoint temperatures.

3. Objective of the Work

Placement is a significant issue in the design automation of very big integrated circuits (VLSI) as it governs the efficiency, size and output of VLSI circuits as well as their reliability. VLSI placement is a NP-hard problem from the computer point of perspective. The current integrating strategy with extremely enormous scopes depends on fixed-line situating impediments with the point of the restrictive region and wire length between the modules. One of the most significant strides in the physical format of the VLSI circuits is the position of a progression of rectangular circuit modules to lessen the complete locale of the association and the greatest interfacing wire length. Many of the modules are not yet fully developed and are often flexible when putting circuit modules (or macro cells) into shape. A circuit module consisting of twelve parts can be placed in a row of twelve components, 2 rows of 5, 3 rows of 8, etc., offering the floor plan designer a choice of conceivable shapes in that module.

Consider an area R with width X and stature Y and a lot of modules $M = \{m_1, m_2, m_3, \cdots, m_n\}$ in which module m_i is a rectangular square with a fixed width X_a, tallness Y_i, and a net rundown N_1 indicating interconnections between modules in M; the issue is to discover a pressing of all modules in the rectangular locale R, so they meet the accompanying conditions:

(1) The module cannot be associated diagonally; it must be parallel to the axis of the coordinate

(2) It is not permitted to overlap one module with any other module

(3) Modules shall be placed within the region R

(4) Any module can be rotated 90° prior to placing

4. Proposed Methodology

4.1. Improved Harmony Search Algorithm-Blended Harmony Search and Particle Swarm Optimization (BHSPS) Algorithm. To optimize the overall placement area routing wirelength and congestion density, it is required to have optimized architecture which was achieved by using the IHS algorithm. To upgrade the exhibition and the viability of the calculations, the successful way is attempted and trying the technique for hybridization between them. The blended harmony search and particle swarm optimization (BHSPS) algorithm is gotten by the hybridization of the harmony search (HS) algorithm and particle swarm optimization (PSO). The hybridization is finished with the work of falling strategy between the harmony search (HS) algorithm and particle swarm optimization (PSO); the falling is done the forward way. HS and PSO are amalgamated because of their individual performances at their best; HS is a very fast algorithm and produces results at a rapid pace whereas PSO has a slow convergence rate and it can produce nearly better solutions. To maintain both speed and accuracy, the BHSPS algorithm is proposed for the purpose of floor planning in VLSI physical design automation to achieve the desired performance. To optimize the overall placement area routing wirelength and congestion density, it is required to have the optimized architecture which was achieved by using the BHSPS algorithm. The IHS algorithm provides a much optimized architecture with a minimum chip area and optimum routing wirelength.

4.2. Process Flow of the BHSPS Algorithm. Figure 1 represents the operational flow of the blended harmony search and particle swarm optimization (BHSPS) algorithm. The algorithm actually comprises of two stages, i.e., operation and simulation. In the first stage, the initial algorithm which is a harmony search (HS) algorithm will be coded and simulated. The HS algorithm will run as per the given parameters like the harmony memory consideration rate (HMCR), pitch adjustment rate (PAR), and band width (BW), and produce the optimal solutions after the required number of iterations, when the stopping criterion is reached. Then, the operation of the first stage will be completed and executed. After the computation of the first stage, the second stage of operation will come into play. The obtained solutions from the first stage will be given as the inputs to the second stage. In the second phase of the blended harmony search and particle swarm optimization algorithm (BHSPS), the standard PSO algorithm will run to get better results than the individual algorithms. HS and PSO will run one after the other in a cascading structure to produce fruitful results. The proposed algorithm is expected to overcome the drawbacks of individual algorithms with its accuracy and desired performance. The novelty of the algorithm lies in its step by step implementation with hybridization of two algorithms using cascading technique and allows standard BMC architectures for the compilation and evaluation of desired VLSI parameters.

4.3. Stages in Blended Harmony Search and Particle Swarm Optimization (BHSPS) Algorithm. The step-by-step procedure of the BHSPS algorithm is noted as follows:

(1) Initialize the memory of the harmony

(2) Set HMCR, PAR, and bandwidth parameters

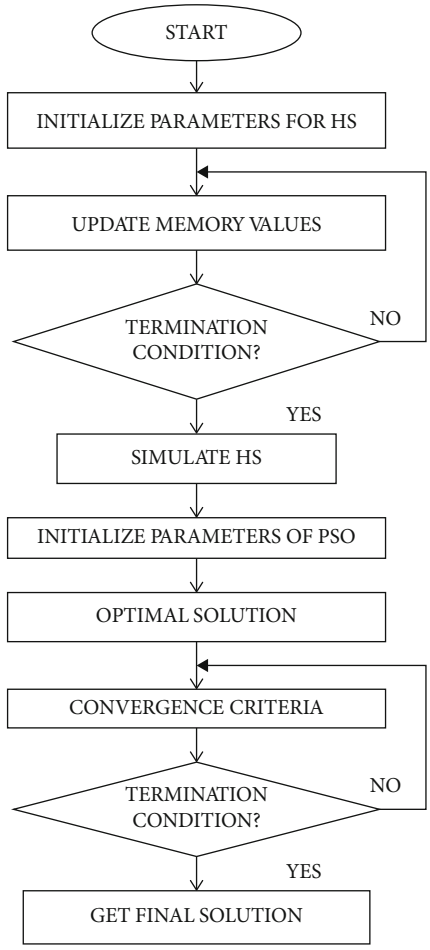

Figure 1: Process flow of the IHS algorithm.

(3) Simulate the algorithm for looking for peace

(4) The abovementioned algorithm solutions are given to the particle swarm optimization (PSO) algorithm as initial values

(5) More optimal solutions will be produced and run by PSO

(6) Until the best solution is found, the process will continue

4.4. HS (Harmony Search) Algorithm. The harmony search (HS) technique is a suggested by Geem et al. for metaheuristic optimization. It imitates the process of musical improvisation in which musicians attempt to discover perfect harmony in an orchestra or band with the help of musical improvisations. Once musicians compose harmonies, the music combos stored in their memory usually try to vary. This algorithmic program was intended to imitate the way that a musician utilizes memory and therefore past experiences that lead to the note that once they have lived alongside the opposites, it leads to the most pleasant harmony. HS is easy to implement and can be easily used to resolve almost any disadvantage which can be designed because an objective is reduced or maximized. The process for discovering optimal or near-optimal alternatives for the tangle is used to conduct such financial exploration for the best state of harmony. A replacement resolution is temporary by 3 exploitation rules. They are

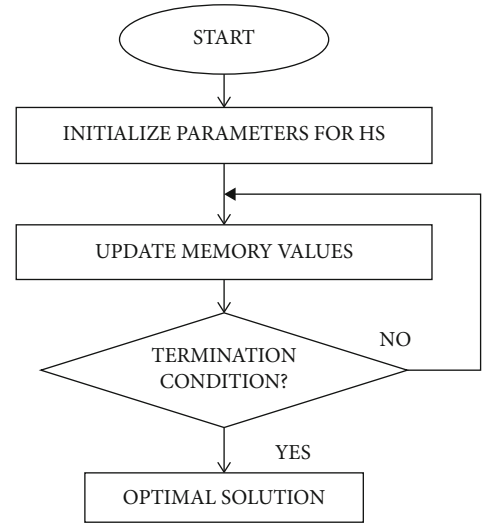

Figure 2: Flowchart of HS.

Table 1: The reference characteristic values of standard MCNCBM circuits.

BM circuit	Standard area	Number of cells	Number of nets
APTE	46.5616	9	97
XEROX	19.3503	10	203
HP	08.8301	11	83
AMI33	1.1564	33	123
AMI49	35.4454	49	408

(1) Memory consideration

(2) Pitch adjustment

(3) Random selection

The HS algorithm main control parameters are

(1) Harmony memory (HM)

(2) Harmony memory size (HMS)

(3) Harmony memory considering rate (HMCR)

(4) Pitch adjustment rate (PAR)

(5) Bandwidth (BW)

4.5. Flowchart of the Harmony Search Algorithm. The flowchart of the harmony search algorithm is shown as follows:

Figure 2 signifies the typical flowchart of HSA by the process of which the procedure starts and also ends. At the start, the underlying congruity memory is produced dependent on the region of use. At the same time, the boundaries of concordance search are characterized. They incorporate

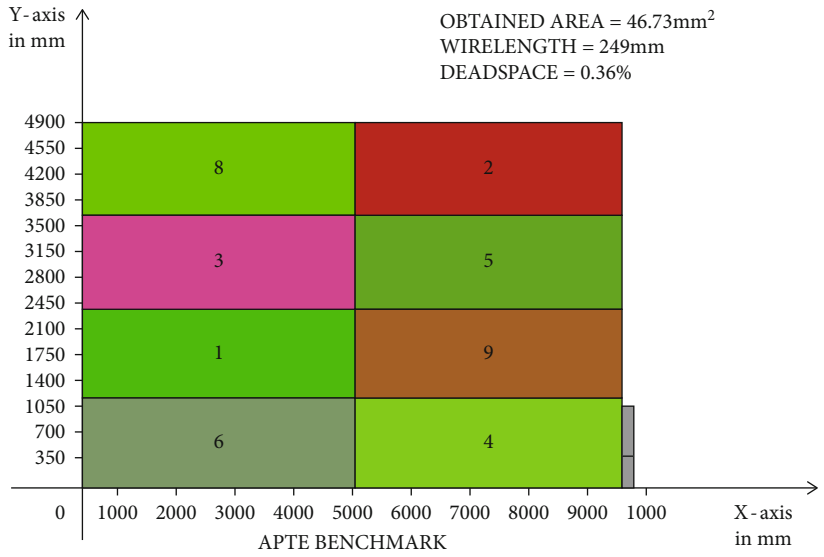

Figure 3: Result of BMC APTE.

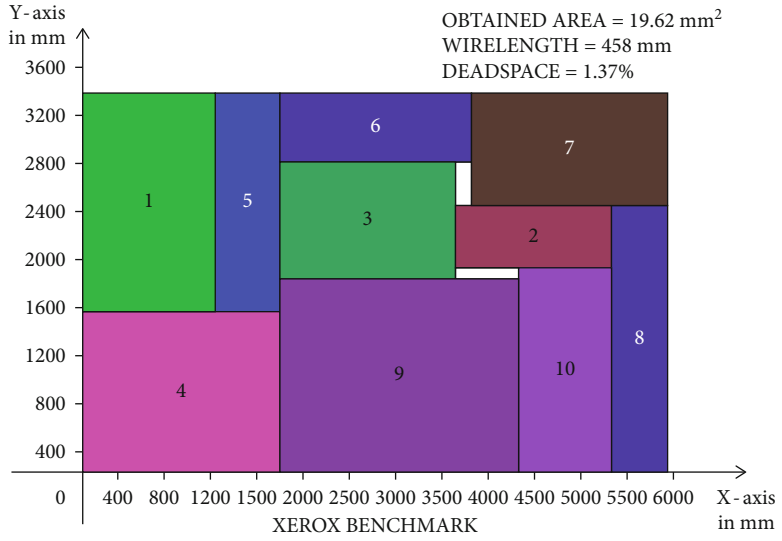

Figure 4: Result of BMC XEROX.

the pitch adjustment rate (PAR) and the consideration rate for harmony memory (HMCR). An irregular number is chosen as a major aspect of a particular cycle. In the event that the arbitrary number is lower than the HMCR, at that point, arbitrarily select a current symphonious, and in the event that a similar irregular number is higher than the PAR, at that point, haphazardly change the pitch inside cutoff points; in any case, randomization would produce new music. The cycle will be proceeded until the halting measure is arrived at, that is, until the group of perfect harmony.

4.6. Step by Step Procedure of the Harmony Search Algorithm

4.6.1. Stage 1: Initialization of the HS (HM) Memory. The initial HS (HM) consists of a number of arbitrary grades to the problems of optimization being considered.

4.6.2. Stage 2: Improvement of the HM's New Arrangement. In view of the HMCR, each part of this arrangement is acquired. The HMCR is considered as the likelihood that a segment will be chosen from the current HM individuals, and henceforth, 1-HMCR is the likelihood of getting it haphazardly.

4.6.3. Stage 3: Now, Updating Your HM (HS). The new phase 2 arrangement is being tried. In the event that it conveys preferable wellness over the HM's most noticeably terrible part, it will supplant it. Else, it will be dropped.

4.6.4. Stage 4. Now, repeat stages 2 and 3 until being in accordance with a predetermined termination condition.

4.7. Definition of Harmony Search Algorithm Parameters. In the HS Algorithm, the utilization of harmony memory is

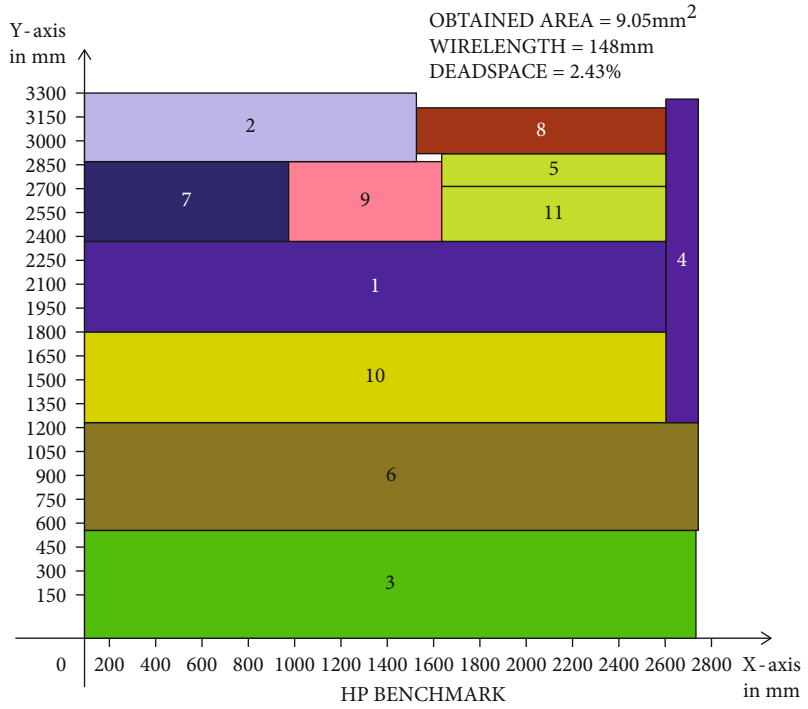

Figure 5: Result of BMC HP.

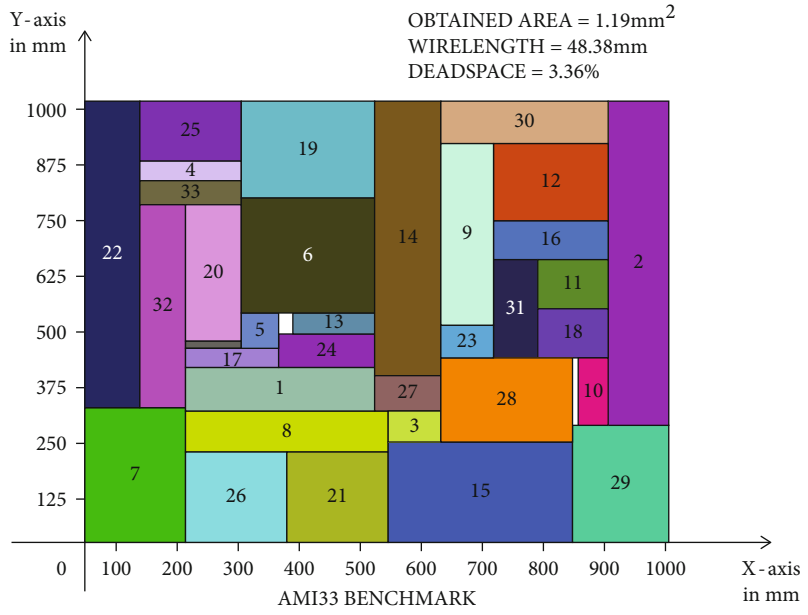

Figure 6: Result of BMC AMI33.

significant and best harmonies will be moved to new harmony memory. It is normally apportioned as a variable called the harmony memory consideration rate (HMCR) to utilize this memory all the more proficiently. In the event that HMCR is low, just not many of the best harmonies will be chosen and it can unite too gradually. On the off chance that HMCR is very high, practically, all the harmonies are utilized in the memory of the congruity, bringing about some unacceptable arrangements because of different harmonies being not all around investigated. HMCR ordinarily differs from 0.7 to 0.95. In this work, HMCR can be considered as 0.9 for better performance of the algorithm over floor planning. Pitch change is controlled by the pitch bandwidth (BW) and pitch adjusting rate (PAR). PAR is allocated to control the level of change, and it for the most part goes from 0.1 to 0.7. Standard is considered as 0.3 and BW as 0.1 for the efficient working of the process.

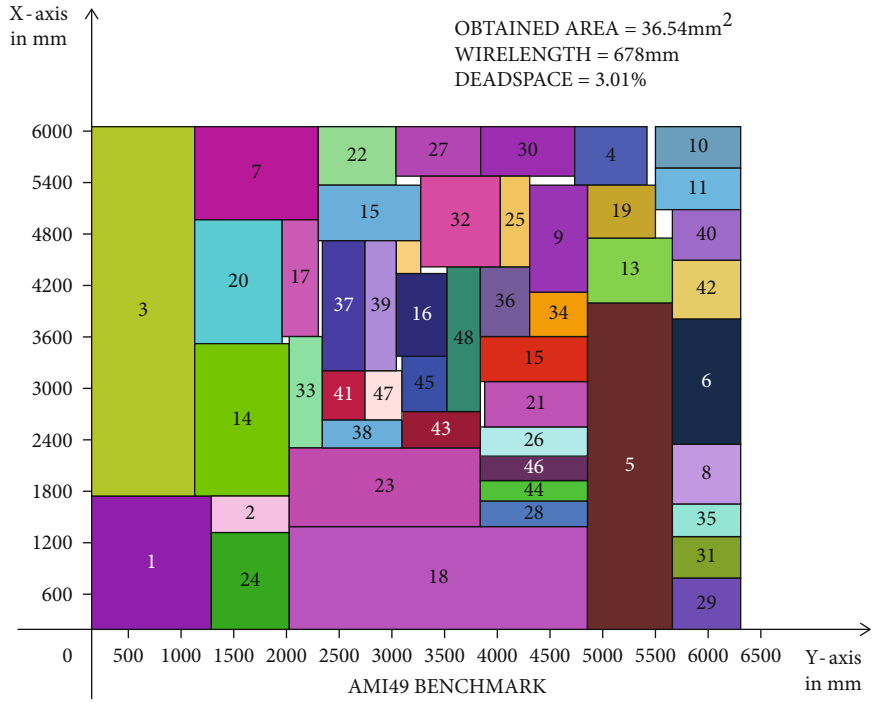

Figure 7: Result of BMC AMI49.

Table 2: Simulation results using GA.

S. no	Benchmark circuit	No. of cells	Standard area (mm^2)	Obtained area (mm^2)	Wire length (mm)
1	APTE	9	46.56	48.21	433
2	XEROX	10	19.35	21.67	989
3	Hp	11	08.83	11.55	184
4	ami33	33	1.15	1.87	198
5	ami49	49	35.44	68.6	4477

Table 3: Simulation results using HSA.

S. no	Benchmark circuit	No. of cells	Standard area (mm^2)	Obtained area (mm^2)	Wire length (mm)
1	APTE	9	46.56	47.40	379
2	XEROX	10	19.35	22.95	913
3	Hp	11	08.83	10.82	142
4	ami33	33	1.15	1.82	197
5	ami49	49	35.44	66.49	3990

5. Results and Discussion

In this paper, all BMC-optimized architectures are generated with the application of the IHS algorithm simulated for 1000 iterations. The optimized result for placement of cells/blocks can be observed by running the MATLAB code with the help of the proposed algorithm with reference to the standard values of MCNCBM circuits. Table 1 shows the reference characteristic values of standard MCNCBM circuits.

The results of the blended harmony search and particle swarm optimization (BHSPS) algorithm to attain better optimized placement results are shown as follows:

Figure 3 indicates the simulation output for the benchmark APTE with 9 cells placed with the help of the blended harmony search and particle swarm optimization (BHSPS) algorithm. This provides outcome values for an ideal area of 45.56 mm^2 and a simulated area with BHSPS of 46.73 mm^2. The ideal area refers to the standard value of

Table 4: Simulation results using PSO.

S. no	Benchmark circuit	No. of cells	Standard area (mm^2)	Obtained area (mm^2)	Wire length (mm)
1	APTE	9	46.56	48.43	376
2	XEROX	10	19.35	20.96	897
3	Hp	11	08.83	10.5	134
4	ami33	33	1.15	1.66	190
5	ami49	49	35.44	47.02	3377

Table 5: Simulation results using the blended harmony search and particle swarm optimization algorithm.

S. no	Benchmark circuit	No. of cells	Standard area (mm^2)	Obtained area (mm^2)	Wire length (mm)	Dead space (%)
1	APTE	9	46.56	46.73	249	0.36
2	XEROX	10	19.35	19.62	458	1.37
3	Hp	11	08.83	9.05	148	2.43
4	ami33	33	1.15	1.19	48.36	3.36
5	ami49	49	35.44	36.54	678	3.01

the benchmark whereas the simulated area refers to the area occupied after application of the optimization algorithm.

Figure 4 indicates the simulation output for the Benchmark XEROX with 10 cells placed with the help of the blended harmony search and particle swarm optimization (BHSPS) algorithm. This has given an ideal area of 18.355 mm^2 and a simulated the area with BHSPS of 19.62 mm^2.

Figure 5 indicates the simulation output for the benchmark HP with 11 cells placed with the help of the blended harmony search and particle swarm optimization (BHSPS) algorithm. This has given an ideal area of 8.983 mm^2 and a simulated area with BHSPS of 9.05 mm^2.

Figure 6 indicates the simulation output for the benchmark AMI33 with 33 cells placed with the help of the blended harmony search and particle swarm optimization (BHSPS) algorithm. This has given an ideal area of 1.115 mm^2 and a simulated area with BHSPS of 1.19 mm^2.

Figure 7 indicates the simulation output for the benchmark AMI49 with 49 cells placed with the help of the blended harmony search and particle swarm optimization (BHSPS) algorithm. This has given an ideal area of 35.144 mm^2 and a simulated area with BHSPS of 36.54 mm^2.

The abovementioned results show the prearrangement of modules between length pivot and even the way and width hub vertical way for the predefined MCNCB circuit. Figure 3 is specifically exhibiting the floorplan of nine modules (APTE) between the characterized x-hub course and y-hub bearing which is gotten in the wake of running the separate MATLAB code for a conceivable number of emphases, the improved placement with the usage of the blended harmony search and particle swarm optimization (BHSPS) algorithm. Similarly, Figures 4–7 represent the floorplans of 33 modules (AMI33), 49 modules (AMI49), and 10 modules (XEROX), respectively.

The block placement by means of the genetic algorithm is carried out on the MCNC benchmark circuit standards yielding area and wirelength along with the fitness function as provided in Table 2. The comparison of the obtained genetic algorithm values with the standard values is mentioned in Table 1. It is observed that the obtained area is better in comparison to standard values. Here, the fitness function is obtained by taking the area and wirelength into consideration. Here, the better area does not mean the highest in block placement; it means the optimal value with respect to the available chip area corresponding to the available wirelength. The fitness function is referred as a certain sort of objective function which summarizes the entire performance as a single parameter of significance to achieve optimal design solution. The fitness function values provided for each benchmark circuit convey how fit the solution is with respective the standard number of cells and also number of nets. It can be notified that with the genetic algorithm, the XEROX benchmark circuit has the highest fitness function which indicates the closeness of the solution towards the overall specification of the desired solution.

The MCNC Benchmark circuits have also been evaluated by the harmonic search algorithm for block placement; the area and wirelength along with the fitness function are presented in Table 3. It can be observed that the obtained area is having an optimal value when compared with standard values for the corresponding benchmark circuits. Here, the fitness function values obtained in consideration with the area and wirelength are better for APTE and HP, indicating the fit element of optimal solution in solving the block placement problem of the work. While dealing with fitness function values, it shall be kept in mind that there is no hard and fast rule of a certain value of the concerned parameters such as the area and wirelength.

Further, the particle swarm optimization algorithm has been investigated for block placement on MCNC benchmark circuits; the obtained area and the corresponding wirelength values along with fitness function values are provided in Table 4. In comparison, the obtained area has optimal values with respect to the standard values. The fitness function

Table 6: Comparison of the proposed method with existing methods.

MCNC benchmark circuit	B^* tree	HGA	SSAA	HS	HPSOHS	BPSO	OBSA	Proposed BHSPS
APTE	46.92	47.01	48.47	48.43	47.44	47.5	47.56	**46.73**
XEROX	19.83	20.14	20.42	20.64	20.1	20.38	20.36	**19.62**
Hp	8.95	9.13	9.40	10.54	9.48	9.58	9.2	**9.05**
Ami33	1.27	1.19	1.26	1.35	1.25	1.21	1.3	**1.19**
Ami49	36.8	37.49	37.76	—	38.5	37.44	—	**36.54**

proves to be an optimal value for the HP benchmark circuit with the value of 0.25 where the area improvement is observed to be 18%. In particle swarm optimization, the particles are arranged randomly by promoting the value obtained for fitness function with respect to the best value of the individual particle and the best value of position of the entire swarm correspondingly, in order to obtain an optimal solution.

After a certain series of investigations carried out based on the genetic algorithm, the harmonic algorithm, and particle swarm algorithm as provided in the previous chapter, now, the computation is carried out based upon the blended algorithms. The choosing of blending is purely based upon the fitness function, as the particle swarm optimization has a leading edge with respect to the genetic harmonic algorithm for the benchmark circuits during block placement; the particle swarm optimization algorithm is blended with the harmonic algorithm; it leads to the blended harmony search and particle swarm optimization (BHSPS) algorithm.

As particle swarm optimization has provided the best values, further, a blended algorithm referred as BHSPS—blended harmony search and particle swarm optimization—algorithm combining both harmony search and particle swarm optimization algorithms has been evaluated for MCNC benchmark circuits and the results are tabulated in Table 5.

After comparing the proposed method with the carried out previous methods in our experimentation, now, a comparison of the area is carried out with the related works in the literature which is tabulated in Table 6. The methods such as B^* tree, hybrid genetic algorithm (HGA), stochastic-based simulated annealing algorithm (SSAA), harmony search (HS), hybrid particle swarm optimization harmony search (HPSOHS), binary particle swarm optimization (BPSO), and order-based simulated annealing (OBSA) have provided the area output values as mentioned in Table 6 for various benchmark circuits which are compared at the end with the proposed BHSPS algorithm. It can be observed that the proposed method has yielded the optimal area values.

6. Conclusion and Future Enhancements

This paper carries out a BHSPS algorithm which is proposed for the advancement of the area utilizing automation in the VLSI circuit design. Through this calculation, we can undoubtedly achieve that the proposed method is quick at the assessment of the territory contrasted with other improvement procedures like PSO and HS, and furthermore, it establishes a smaller number of stages and steps. This technique is helpful for designing VLSI ICs with less space and fast operation with the help of artificial intelligence and data science. The proposed algorithm can estimate performance parameters like the area, wirelength, and dead space but not cover the characteristics like the power required, clock speed, and compatibility. As an end, the optimized placement region got through this strategy and we can contrast it and the standard zone of MCNC BM circuits. The solid examination tends to be reasoned that the proposed calculation is effective in accomplishing the objective and goal of optimizing placement accordingly delivering better foundation for the VLSI design. With the execution of this proposed calculation, an extensive decrease of the dead space is accomplished along these lines making it more significant in different uses of examination in the territory of VLSI plan. The proposed technique can be used to estimate the area, wirelength, and dead space for any other architectures and also helpful for analyzing the reduction of the area and operational time of the chip.

Data Availability

The processed data are available upon request from the corresponding author.

Conflicts of Interest

The authors declare that they have no conflicts of interest to report regarding the present study.

Authors' Contributions

Shaik Karimullah did the conceptualization and methodology. D. Vishnuvardhan did the visualization and supervision. Muhammad Arif did the writing—original draft. Vinit Kumar Gunjan did the investigation. Fahimuddin Shaik did the analysis and validation. Kazy Noor-e-alam Siddiquee did the editing.

References

[1] I. Ratkovi, O. Palomar, M. Stani, O. Unsal, A. Cristal, and M. Valero, "Physical vs. physically-aware estimation flow: case study of design space exploration of adders," in *2014 IEEE Computer Society Annual Symposium on VLSI*, Tampa, Florida, USA, 2014.

[2] S. Karimullah and D. Vishnuvardhan, "Experimental Analysis of Optimization Techniques for Placement and Routing in Asic Design," Springer Nature Singapore Pte Ltd., 2020.

[3] S. Pinge, R. K. Nain, and M. Chrzanowska-Jeske, "Fast floorplanning with placement constraints," in *2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS)*, Cusco, Peru, 2013.

[4] Iyengarand Lakhshmi Shrinivasn, "Power, performanceand area optimization of I/O design," in *International Conference on Inventive Research in Computing Applications (ICIRCA 2018)*, Coimbatore, Tamil Nadu, India, 2018.

[5] S. Karimullah and D. Vishnu Vardhan, "Iterative analysis of optimization algorithms for placement and routing in Asic design," in *ICDSMLA 2020, Lecture Notes in Electrical Engineering 601*, Springer Nature Singapore Pte Ltd., 2020.

[6] J.-M. Lin, W.-Y. Cheng, C.-L. Lee, and R. C. J. Hsu, "Voltage island-driven floorplanning considering level shifter placement," in *17th Asia and South Pacific Design Automation Conference*, pp. 443–448, Sydney, Australia, 2012.

[7] K. Shaik, D. Vishnu Vardhan, and S. J. Basha, "Floorplanning for Placement of Modulesin VLSI Physical Design Using Harmony Search Technique," in *ICDSMLA 2020, Lecture Notes in Electrical Engineering 601*, Springer Nature Singapore Pte Ltd., 2020.

[8] Y.-F. Chen, C.-C. Huang, C.-H. Chiou, Y.-W. Chang, and C.-J. Wang, *Routability-Driven Congestion-Aware Macro Placement*, 2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, CA, USA, 2014.

[9] S. Karimullah and D. Vishnuvardhan, "A review paper on optimization of placement and routing techniques at NC'e-TIMES # 1.0 IN 2018," *IJET*, vol. 1, p. 2395-1303, 2018.

[10] J. Z. Yan, N. Viswanathan, and C. Chu, "Handling complexities in modern large-scale mixed-size placement," in *Proceedings of the 46th Annual Design Automation Conference*, pp. 436–441, San Francisco, CA, 2009.

[11] S. M. Ahmed, B. Kovela, and V. K. Gunjan, "IoT based automatic plant watering system through soil moisture sensing—a technique to support farmers' cultivation in rural India," in *Advances in Cybernetics, Cognition, and Machine Learning for Communication Technologies*, pp. 259–268, Springer, Singapore, 2020.

[12] S. Karimullah and D. V. Vardhan, "Pin density technique for congestion estimation and reduction of optimized design during placement and routing," *Applied Nanoscience*, pp. 1–10, 2022.

[13] P. S. Prasad, B. Sunitha Devi, M. Janga Reddy, and V. K. Gunjan, "A survey of fingerprint recognition systems and their applications," in *International Conference on Communications and Cyber Physical Engineering 2018*, pp. 513–520, Springer, Singapore, 2019.

[14] B. Mokhlesabadifarahani and V. K. Gunjan, *EMG Signals Characterization in Three States of Contraction by Fuzzy Network and Feature Extraction*, Springer, 2015.

[15] M. Samaranayake, H. Ji, and J. Ainscough, "Module placement based on hierarchical force directed approach," in *2009 3rd International Conference on Signals, Circuits and Systems (SCS)*, pp. 1–6, Medenine, Tunisia, 2009.

[16] M. D. Ansari, V. K. Gunjan, and E. Rashid, *On Security and Data Integrity Framework for Cloud Computing Using Tamper-Proofing*, In ICCCE 2020, Springer, Singapore, 2021.

[17] K. Prasanna and M. Seetha, "A doubleton pattern mining approach for discovering colossal patterns from biological dataset," *International Journal of Computer Applications*, vol. 119, no. 21, pp. 41–47, 2015.

[18] P. Sivaranjani, S. Athappan, E. Devi, and M. Shanmugam, "Optimization of thermal aware VLSI non-slicing floorplanning using hybrid particle swarm optimization algorithm-harmony search algorithm," *Circuits and Systems*, vol. 7, no. 562-573, 2016.

[19] M. Usman, M. Wajid, M. Z. Shamim, M. D. Ansari, and V. K. Gunjan, "Threshold detection scheme based on parametric distribution fitting for optical fiber channels," *Recent Advances in Computer Science and Communications (Formerly: Recent Patents on Computer Science)*, vol. 14, no. 2, pp. 409–415, 2021.