WILEY | Hindawi

Research Article

Energy-Efficient UART Design on FPGA Using Dynamic Voltage Scaling for Green Communication in Industrial Sector

D. Haripriya [ID],[1] **Keshav Kumar** [ID],[2] **Anurag Shrivastava** [ID],[3]
Hamza Mohammed Ridha Al-Khafaji [ID],[4] **Vishal Moyal** [ID],[5] **and Sitesh Kumar Singh** [ID][6]

[1]*Department of ECE, SRM Institute of Science and Technology, Ramapuram Campus, Chennai 600089, India*
[2]*University Institute of Computing, Chandigarh University, Punjab, India*
[3]*Department of Electronics and Communication Engineering, Lakshmi Narain College of Technology and Science, Indore, 453111 Madhya Pradesh, India*
[4]*Biomedical Engineering Department, Al-Mustaqbal University College, 51001 Hillah, Babil, Iraq*
[5]*Department of Electrical Engineering, SVKMs Institute of Technology, Dhule, M.S 424002, India*
[6]*Department of Civil Engineering, Wollega University, Nekemte, Oromia, Ethiopia*

Correspondence should be addressed to Sitesh Kumar Singh; sitesh@wollegauniversity.edu.et

In the present scheme of the world, the problem of shortage of power is seen across the world which can be a vulnerability to various communication securities. The scope of proposed research is that it is a step towards completing green communication technology concepts. In order to improve energy efficiency in communication networks, we designed UART using different nanometers of FPGA, which consumes the least amount of energy. This shortage is happening because of expanding of industries across the world and the rapid growth of the population. Therefore, to save the power for our upcoming generation, the globe is moving towards the concept and ideas of green communication and power-/energy-efficient gadget. In this work, a power-efficient universal asynchronous receiver transmitter (UART) is implemented on 28 nm Artix-7 field-programmable gate array (FPGA). The objective of this work is to reduce the power utilization of UART with the FPGA device in industries. To do this, the same authors have used voltage scaling techniques and compared the results with the existing FPGA works.

1. Introduction

In recent times, it has been observed that the whole globe is suffering from one serious problem which is power deficiency. This is happening all over the globe due to the vast increase in the population as well as industrialization. Therefore, to save power for our upcoming generation, the whole world is going towards the concept of energy-/power-efficient gadgets and green communication technology. The "green communication" refers to methods for conserving energy resources for future generations without affecting current generation use. As a result, UART may be useful in developing green communication concepts. Our research work is a step towards fulfilling the designs of green communication technologies. The green communication enables

totally better idea of working, interacting, and cooperating, allowing corporations to go further while reducing pollution, greenhouse gas emissions, and power usage. Many organizations are reluctant to make the switch due to the high initial expenditures. We created UART utilizing various nanometers FPGA, which consumes the least amount of energy, in order to minimize energy usage in communication networks. UART is an abbreviation for universal asynchronous receiver transmitter. UART has a frequency of 1 GHZ, a responsibility cycle of 50%, and a time period of 1 ns. The responsibility cycle of a signal is the amount of time it is used. The power and duty cycle relationship = (PW/T) 100, where D is the responsibility cycle, PW is the pulse width, and T is the signal's time period. In UART, data is sent at a particular frequency called Baud rate. In the UART time

technique, the data is sampled when the baud rates of the receiver and transmitter are properly aligned. In the process of data transfer, the data is sent in an irregular way via UART connection. That is, no clock signal is necessary to transfer data from UART A to UART B. As a result, UART may be useful in developing green communication concepts. The hardware circuit of UART device is associated with microcontrollers, laptops, and CPU of a computer. Sometimes it can be dedicated to an integrated circuit (IC). Despite a lot of new communicating ideas, UART communication is most preferred for serial communication. This is because UART devices are easily integrable, and it only uses two wires to perform the serial communication, which is given in Figure 1.

The data transfer in UART takes place in the form of packets; i.e., the UART sends data to another UART in the form of packets of bits. Since the communication of data in UART transfers data in an asynchronous manner, that is, for sending data from UART A to UART B, no clock signal is required. Therefore, UART can be beneficial for promoting the ideas of green communication. If we compare the proposed method with existing methods in this research, voltage scaling is used to calculate power, and the findings of the study are compared to previous methodologies. It has been found that researchers have employed a variety of strategies to minimize power consumption in previous studies, yet consumption can still be lowered. The existing works done on UART implementation on FPGA to promote the ideas of green communication are explained in Section 2.

The present article has been planned into seven sections. Section 1 describes the introduction of UART with green communication. Section 2 puts light on related work. The implementation setup and methodology have been mentioned in Section 3. Section 4 described the thermal properties for different voltage values. The power calculation of UART has been discussed in Section 5. Finally, Section 6 portrays the conclusion and possible future works based on the proposed framework.

1.1. Field-Programmable Gate Array (FPGA). Unlike the other microcontrollers, FPGAs are also those gadgets that are composed up of semiconductor materials [2–4]. These devices work similarly to the other microcontrollers but have one distinguished property which makes FPGA more convenient than the other microcontrollers. The major and the most important advantage of using FPGAs is these [5] can be reprogrammed after its manufacturing. The feature of being reprogrammed makes FPGAs handier and convenient to be used than the other microcontrollers [6, 7]. The major building blocks of FPGAs are look-up tables (LUTs), configurable logic blocks (CLBs), flip-flops, input/output (I/O) devices, memory devices, and buffers [8]. The building components of FPGAs are shown in Figure 2. FPGA devices are used for performing the green communication too. Green communication is the techniques in which we tend to save the energy resources for our future generation without compromising the use of present generation. The FPGA version of green computing model of UART is shown in Figure 3.

2. Literature Work

The authors created an energy-efficient instruction register for integrating green communication on Virtex 4, Virtex 5, and Virtex 6 FPGAs [9]. As a result, while much work has been done to incorporate the ideas of green communication and energy-/power-efficient devices for future generations on CU with various FPGAs, no work has been done to implement the CU circuit on Kintex-7 ultrascale FPGA, so in this work, the CU circuit is being designed on Kintex-7 ultrascale FPGA to promote green communication techniques.

To provide a high-performance FIFO for the CPU while reducing power usage, Saxena et al. [10] employed voltages and frequency scaling techniques to create FPGA-based FIFO architecture. They altered frequency from 20 MHz to 250 MHz while keeping the voltage constant at 2.3 volt, while for the other experiments, they maintained the frequency constant while varying voltages from 1 volt to 2.3 volt. They concluded that the voltage scaling reduces power usage by 95.79 percent, whereas frequency scaling reduces power consumption by 4.38 percent.

Kumar et al. [1] proposed a Spartan-3 and Spartan-6 field-programmable gate arrays that are used to create a low-power transceiver (FPGA). As a transceiver, a universal asynchronous receiver transmitter (UART) device is employed. The power analysis findings are aimed on Spartan-3 and Spartan-6 FPGAs, and the implementation of UART is achievable with EDA tools named Xilinx 14.1. By altering the voltage supply, the change of different power of chips built on FPGA is noticed, for example, input/output (I/O) power consumption, leakage power absorption, signal power utilization, logic power utilization, and the use of complete power. This study examines how voltage changes affect the power consumption of the UART on Spartan-3 and Spartan-6 FPGA devices. Spartan-6 is proven to be more power efficient as the voltage supply is increased.

In the current international situation, the global energy crisis is a very serious concern. The energy crisis in India, as well as a scarcity of natural resources such as crude oil, coal, and other minerals, has an impact on the country's economy [11]. Global demand for energy has risen dramatically as a result of population increase and industrial development. So, in order to save energy, we are creating a UART with FPGAs that uses less power. The universal asynchronous receiver transmitter, or UART, is a serial data transfer device. For data transfer, just two wires are required in UART. Not only that, but there are no clock signals needed to run UART. When the voltage is at its maximum, the UART creates less noise and interference, allowing the signal to travel further [12, 13]. The writers created an electronic control unit (ECU) on FPGA to control the vehicle's system. For parallel work, the reduced instruction set computer (RISC) machine (ARM) processor is utilized in conjunction with FPGA [14].

Kumar and Pandey [14] used stub series terminated logic (SSTL) IO with three distinct FPGAs with varying nanometer (nm) gate sizes: 28 nm SP AR TAN-7, 20 nm KINTEX-7 ultrascale, and 16 nm ZYNQ ultrascale+. The model was created and implemented using the VIV ADO
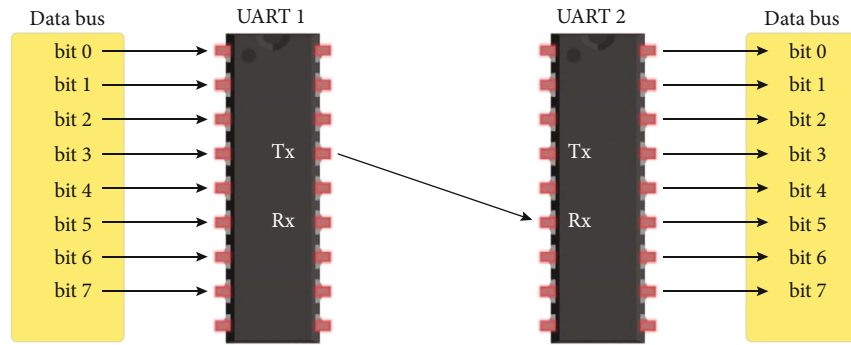
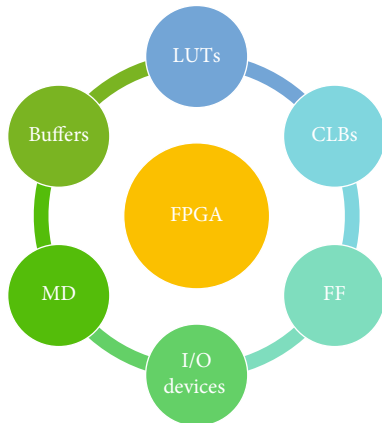FIGURE 1: Serial communication in UART [1].
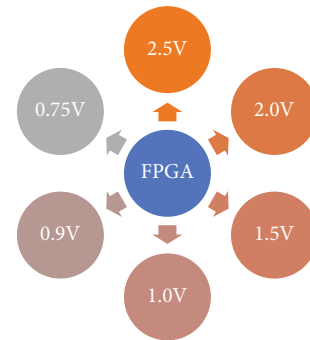

FIGURE 2: Building blocks of FPGAs.

FIGURE 3: Green computing model of UART.

FIGURE 4: Voltage range for power calculation.

simulate and analyze the control unit. The energy consumed of the control unit is examined for various frequency values, and it is discovered that as the frequency grows, so does the total power consumption. As a result, the control unit is better suited to operate at low frequencies in order to reduce power consumption. In addition, lowering the device operating frequency of the control unit from 5 GHz to 100 MHz reduces the overall power usage by 36%.

3. Implementation Setup and Methodology

The implementation and simulation of UART protocol with FPGA are done on XILINX ISE design suite [5, 15]. The results of power consumption of UART are observed for various input voltage ranging from 2.5 V to 0.75 V which is shown in Figure 4. The power calculation is done by X power analyzer tool [16, 17].

4. Thermal Properties for Different Voltage Values

The three thermal possessions are related to FPGA which are termed such as

(i) Effective thermal resistance to air (effective TJA) (^{o}C/W). It shows how the power is distributed to ambient air. For all the value of voltage it is 3.3°C/ W [18–20]

ISE tool. According to the power study, the 16 nm ZYNQ ultrascale+ requires the most power for operation with SSTL18 I IO, while the 28 nm SP AR TAN-7 requires the least power for operation with SSTL135 IO, and the 20 nm KINTEX-7 ultrascale sits in the middle of both of these devices.

Pandey et al. [5] proposed that a power-efficient control unit (CU) is designed and implemented on the Kintex-7 ultrascale FPGA. The VIVADO HLx design suite is used to
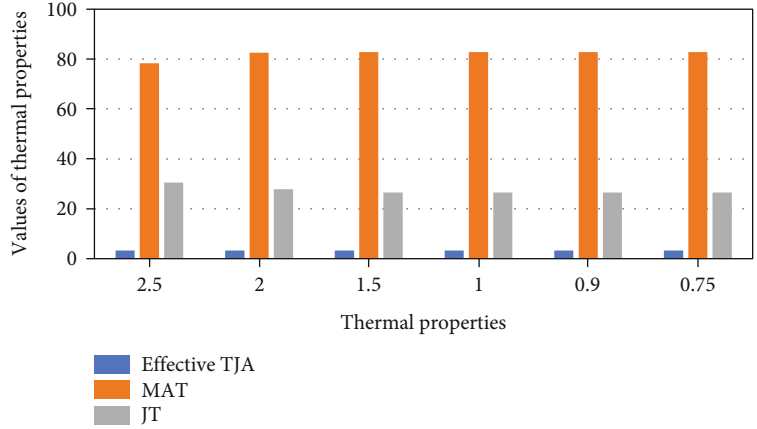
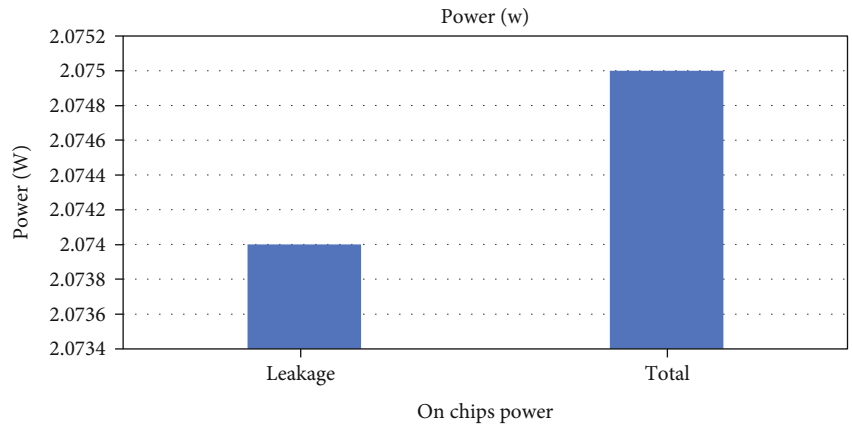FIGURE 5: Thermal properties for different voltage values.
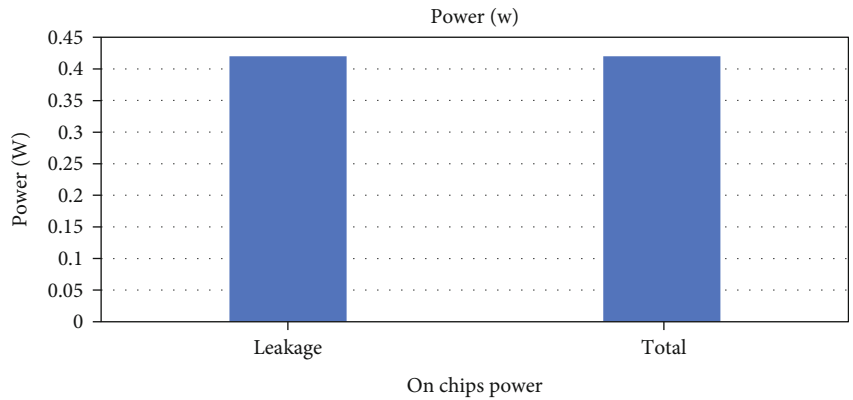

FIGURE 6: TP for the voltage of 2.5 V.

FIGURE 7: TP for the voltage of 2.0 V.

(ii) Maximum (max) ambient temperature (MAT) (°C). Under operating conditions, it is expressed as the temperature around the FPGA [21–23]

(iii) Junction temperature (JT) (°C). It is called as the operational temperature of the FPGA [5, 24]. It is

the aggregate total on chips power, effective TJA, and MAT [5]

The thermal properties with all the voltage range of values for UART protocol for Artix-7 FPGA are represented in Figure 5.
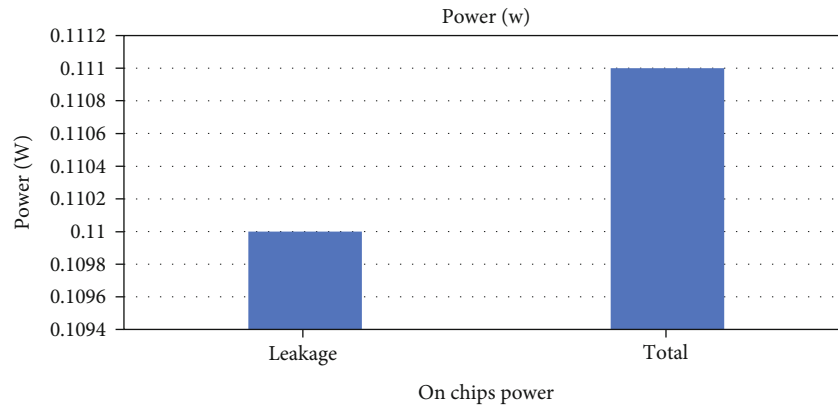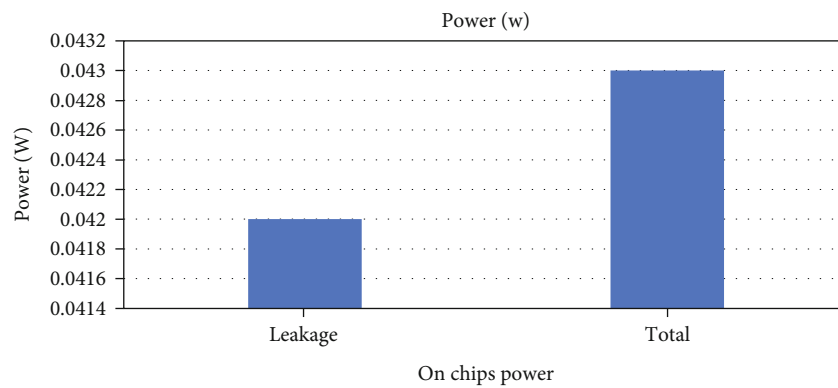
FIGURE 8: TP for the voltage of 1.5 V.
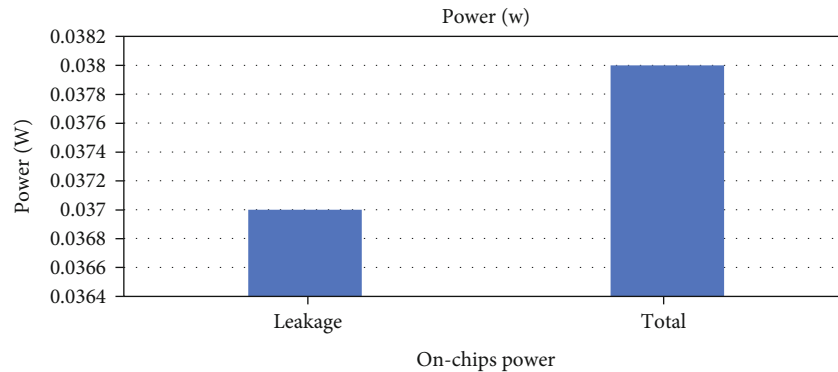

FIGURE 9: TP for the voltage of 1.0 V.

FIGURE 10: TP for the voltage of 0.9 V.

5. Power Calculation of UART

The total power (TP) dissipation of UART protocol on FPGA device is the sum up of the dynamic power (DP) of the device and the static power (SP) of the device [25, 26]. Although there are a large number of innovative communication concepts, serial communication via UART is still the most popular. This is due to the ease with which UART devices may be integrated and the fact that serial communication is accomplished with only two wires. The dynamic power is the power calculated when there is any switching in the device, whereas the static power is the steady-state power of the device. In a FPGA device the clock, logic, IO, and signal power are the device static power, whereas the leakage power is the device dynamic power [3, 4]. Whenever the transmission rates of the transmitter and the receiver are suitably aligned, the data is sampled using the UART time approach. Microcontrollers, laptops, and a computer's CPU are all connected to the physical circuit of a UART device. Sometimes, it can be dedicated to an integrated circuit (IC).
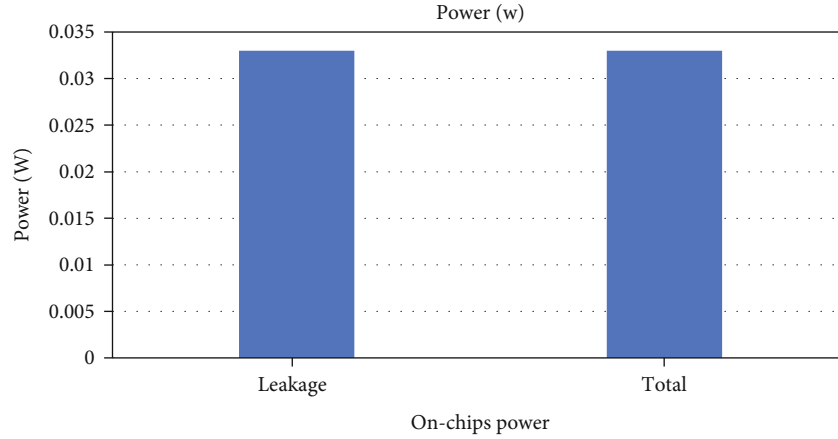
$$TP = DP + Sp. \qquad (1)$$
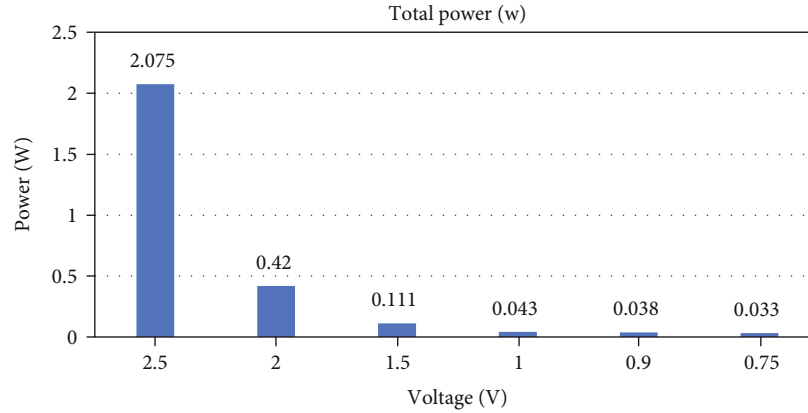
FIGURE 11: TP for the voltage of 0.75 V.

FIGURE 12: TP for all voltage values.

TABLE 1: Comparative power analysis.

S. no	Reference	FPGA	Power (W)
1.	[9]	Virtex 6	17.226
2.	[10]	Virtex 6	2.244
3.	[1]	Virtex 6	1.293
4.	[11]	Virtex 6	45.334
5.	[12]	Kintex 7	1.804
6.	[13]	Virtex 4	0.177
7.	[14]	Virtex 6	1.407
8.	[27]	Spartan 6	0.296
9.	[28]	Spartan 6	0.297
10.	[4]	Spartan 3	0.080
11.	This work	Artix 7	0.033

5.1. Power Analysis for 2.5 V Voltage. When the voltage is set to 2.5 V for the power calculation, then, there is no SP consumption for the FPGA device; that is, the SP is 0.00 W. On the other hand, the DP, which is the leakage power consumption, is 2.074 W. Hence, the TP of the UART for 2.5 V is 2.075 W. The TP for the voltage of 2.5 V is shown in Figure 6.

5.2. Power Analysis for 2.0 V Voltage. When the voltage is set to 2.0 V, the TP consumption of the device becomes 0.420 W. For 2.0 V voltage, the leakage power is 0.420 W. There is no consumption of SP for the device at this level of voltage. The TP at this voltage value is equivalent to the leakage power of the FPGA. The power consumption for 2.0 V voltage is represented in Figure 7.

5.3. Power Analysis for 1.5 V Voltage. For the voltage value of 1.5 V, the device DP is 0.110 W, and there is no power utilization of SP. Hence, the TP for this voltage becomes similar to the DP. The TP utilization for this voltage is 0.111 W. The power consumption for this value of voltage is described in Figure 8.

5.4. Power Analysis for 1.0 V Voltage. When the voltage is regulated to 1.0 V for the power calculation, then, there is no SP consumption for the FPGA device that is the SP is 0.00 W. On the other hand, the DP, which is the leakage power consumption, is 0.042 W. Hence, the TP of the UART for 2.5 V is 0.043 W. The TP for the voltage of 1.0 V is shown in Figure 9.

5.5. Power Analysis for 0.9 V Voltage. When the voltage is tweaked to 0.9 V, the TP consumption of the device becomes
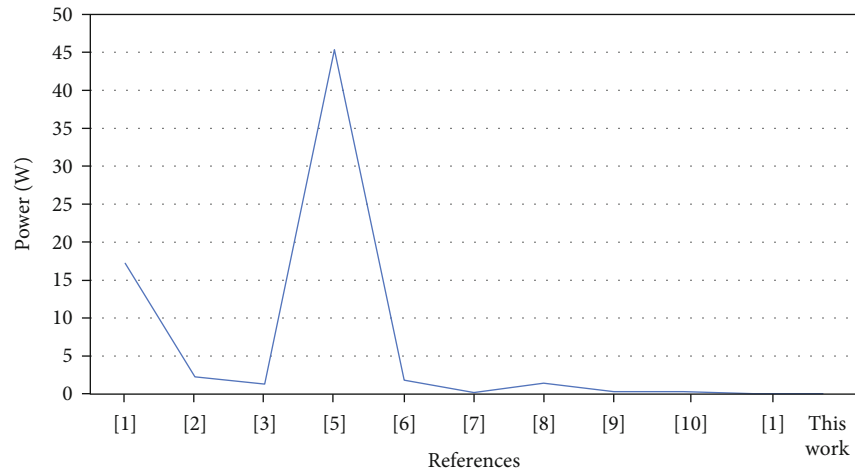
FIGURE 13: Total power comparisons.

0.038 W. For 0.9 V voltage, the leakage power is 0.037 W. There is no consumption of SP for the device at this level of voltage. The TP at this voltage value is equivalent to the leakage power of the FPGA. The power consumption for 0.9 V voltage is represented in Figure 10.

5.6. Power Analysis for 0.75 V Voltage. When the voltage is regulated to 0.75 V for the power calculation, then, there is no SP consumption for the FPGA device; that is, the SP is 0.00 W. On the other hand, the DP, which is the leakage power consumption, is 0.033 W. Hence, the TP of the UART for 0.75 V is 0.033 W. The TP for the voltage of 0.75 V is shown in Figure 11.

By analyzing the power, it can be seen that as the value of voltage drops, the power consumption gets decreased. The power consumption is higher for 2.5 V voltage and lower for 0.75 V voltage. The TP consumption for all the value of voltages is represented in Figure 12.

5.7. Comparative Power Analysis. From the related work section, it is observed that a lot of work has been done by the researchers to optimize the power consumption of the UART protocol. The voltage scaling method is used to calculate power, and the findings of the study are compared to previous methodologies. It has been found that researchers have employed a variety of strategies to minimize power consumption in previous studies, yet consumption can still be lowered. In this section, we have compared our best results with the existing work in recent times. In this work, we have found that the power consumption of UART is optimized when the input supplied voltage is 0.75 V. Of all the rest of the values of voltages, the power consumption is higher as it is explained in Section 4. The comparative power analysis of our work with the other existing work is described in Table 1.

From Table 1, it can be seen that in [9] using the capacitance scaling technique, the TP consumption is 17.226 W. When the thermal characteristics are adjusted in [10], the power usage is 2.244 W. On the Virtex-6 FPGA, TP consumption reaches 1.2936 W in [1]. By adjusting the capacitance at the output load in [11], the power dissipation is increased to 45.334 W. [12] uses multiple IO standards to reduce the TP consumption on the Kintex-7 FPGA to 1.804 W. The power dissipation in [13] is 0.177 W due to the utilization of numerous FPGAs with varied nanoscale technologies. The power consumption of UART is 1.407 W in [14] when various IO standards are used. On the Spartan-6 FPGA, the UART power reaches 0.296 W in [27]. Using the frequency scaling technique, [28] determined that the power usage of the UART is 0.297 W. In [4] with the idea of voltage scaling, the power consumption of UART is 0.080 W on Spartan-3 FPGA. But in our work, the power of UART reaches to 0.033 W, by applying the voltage scaling approach on 28 nm Artix-7 FPGA. The comparison of the total power consumption of our proposed method with the existing techniques is shown in Figure 13.

The problem of energy shortage is affecting the entire planet. This is occurring as a result of massive population and industry expansion throughout the world. As a result, the entire globe is attempting to embrace green communication technology and power/energy saving gadgets. This project is only focused on these technologies. The dynamic power is computed when the device is switched on; meanwhile, the static power is determined when the device is in its stable state. At 2.0 V voltage, there is no use of SP by the gadget. At this voltage level, the TP is equal to the FPGA's leakage power. When the voltage is controlled at 1.0 V for power calculations, the FPGA device consumes no SP, resulting in an SP of 0.00 W. When the voltage is increased to 0.9 V, the device's TP consumption drops to 0.038 W. The leakage power at 0.9 V voltage is 0.037 W. When looking at the power, it can be seen that when the voltage value decreases, the power consumption increases.

6. Conclusion and Future Scope

In the work introduced in this research, we have implemented UART on 28 nm Artix-7 FPGA for green communication. The analysis and simulation are implemented on XILINX design suite, and the power calculation is done

through X power analyzer. The purpose of this research is to lower the power usage of UART in companies using an FPGA device. The scientists employed voltage scaling techniques to accomplish this and compared the findings to previous FPGA work. In this work, the power calculation is done by scaling voltage, and the results of the analysis are compared with the existing techniques. It is observed that in the existing works, researchers have used a lot of different techniques to reduce the power consumption, but the consumption can be reduced up to 0.080 W of power in [1]. In the other work, the power consumption is relatively more than the power consumption in [1]. From comparing our results with [1], it is found that in our proposed design, the power consumption is reduced up to 58.75%. The implementation of UART can be done on the upcoming advanced ultrascale and ultrascale+ FPGAs in future. Later these designs can be converted into ASIC design which is handier and portable than FPGAs.

Data Availability

Conflicts of Interest

Acknowledgments

References

[1] K. Kumar, B. Pandey, A. K. Pandit, Y. A. El-Ebiary, S. A. Mjlae, and S. Bamansoor, "Design of low power transceiver on Spartan-3 and Spartan-6 FPGA," *International Journal of Innovative Technology and Exploring Engineering*, vol. 8, no. 12S2, pp. 27–30, 2019.

[2] V. Jagota, M. Luthra, J. Bhola, A. Sharma, and M. Shabaz, "A secure energy-aware game theory (SEGaT) mechanism for coordination in WSANs," *International journal of swarm intelligence research*, vol. 13, no. 2, pp. 1–16, 2022.

[3] K. Kumar, K. R. Ramkumar, and A. Kaur, "A design implementation and comparative analysis of advanced encryption standard (AES) algorithm on FPGA," in *2020 8th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions) (ICRITO)*, pp. 182–185, Noida, India, 2020.

[4] A. Shrivastava, A. Rizwan, N. S. Kumar et al., "VLSI implementation of green computing control unit on Zynq FPGA for green communication," *Wireless Communications and Mobile Computing*, vol. 2021, Article ID 4655400, 10 pages, 2021.

[5] B. Pandey, K. Kumar, A. Batool, and S. Ahmad, "Implementation of power-efficient control unit on ultra-scale FPGA for green communication," *3C Tecnología*, vol. 10, no. 1, pp. 93–105, 2021.

[6] R. Hartenstein, "Basics of reconfigurable computing," in *Designing Embedded Processors*, pp. 451–501, Springer, Dordrecht, 2007.

[7] G. V. Bharadwaj, A. V. Krishna, M. S. Krishna, and T. Akhil, *Novel Technique on Channel Security using UART*, 2014.

[8] T. Kumar, B. Pandey, T. Das, and B. S. Chowdhry, "Mobile DDR IO standard based high performance energy efficient portable ALU design on FPGA," *Wireless Personal Communications*, vol. 76, no. 3, pp. 569–578, 2014.

[9] M. T. Siddiquee, K. Kumar, P. Pandey, and A. Kumar, "Energy efficient instruction register for green communication," *International Journal of Engineering and Advanced Technology (IJEAT)*, vol. 8, no. 2S2, 2019.

[10] A. Saxena, A. Bhatt, P. Gautam, P. Verma, and C. Patel, "High performance FIFO design for processor through voltage scaling technique," *Indian Journal of Science and Technology*, vol. 9, no. 46, 2016.

[11] D. Nandy, "Energy crisis of India: in search of new alternatives," *Journal of Business & Financial Affairs*, vol. 5, no. 4, pp. 1–6, 2016.

[12] K. Kumar, A. Kaur, S. N. Panda, and B. Pandey, "Effect of different nanometer technology-based FPGA on energy efficient UART design," in *2018 8th International Conference on Communication Systems and Network Technologies (CSNT)*, pp. 1–4, Bhopal, India, 2018.

[13] K. Kumar, A. Kaur, B. Pandey, and S. N. Panda, "Low power UART design using different nanometer technology-based FPGA," in *2018 8th International Conference on Communication Systems and Network Technologies (CSNT)*, pp. 1–3, Bhopal, India, 2018.

[14] J. Pérez, M. Alcázar, J. M. Velasco, J. A. Cabrera, and J. J. Castillo, "Low-cost FPGA-based electronic control unit for vehicle control systems," *Sensors*, vol. 19, no. 8, p. 1834, 2019.

[15] T. Kumar, B. Pandey, S. H. Mussavi, and N. Zaman, "CTHS based energy efficient thermal aware image ALU design on FPGA," *Wireless Personal Communications*, vol. 85, no. 3, pp. 671–696, 2015.

[16] T. Das, B. Pandey, M. A. Rahman, and T. Kumar, "SSTL based green image ALU design on different FPGA," in *2013 International Conference on Green Computing, Communication and Conservation of Energy (ICGCE)*, pp. 146–150, Chennai, India, 2013.

[17] A. Shrivastava and S. K. Sharma, "Various arbitration algorithm for on-chip (AMBA) shared bus multi-processor SoC," in *2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS-2016) organized by MNIT*, pp. 1–7, Bhopal, India, 2016.

[18] "AMBA AXI bus verification technique," *International Journal of Applied Engineering Research*, vol. 10, no. 24, pp. 44178–44182, 2015.

[19] "Reliable routing architecture and algorithm for network-on-Chip," *Journal of Electronic Design Technology*, vol. 6, no. 3, pp. 40–48, 2015.

[20] D. S. Ushakov, I. I. Haiovyi, I. M. Minich, and K. D. Didenko, "Transnational players in tourism: regional features of functioning," *Geojournal of Tourism and Geosites*, vol. 32, no. 4, pp. 1425–1432, 2020.

[21] A. K. Singh, A. Shrivastava, and G. S. Tomar, "Design and implementation of high performance AHB reconfigurable arbiter for onchip bus architecture," in *IEEE International Conference on Communication Systems and Network Technologies, organized by SMVDU*, pp. 455–459, Katra, India, 2011.

[22] A. Shrivastavastava, G. S. Tomar, and K. K. Kalra, "Efficient design and performance analysis for AMBA bus architecture

based system-on-chip," in *IEEE International Conference on Computational Intelligence and Communication Systems organized by R.G.P.V*, pp. 656–660, Bhopal, India, 2010.

[23] D. M. Pham and S. M. Aziz, "FlexiS—a flexible sensor node platform for the internet of things," *Sensors*, vol. 21, no. 15, p. 5154, 2021.

[24] K. Kumar, A. Kaur, and K. R. Ramkumar, "Effective data transmission with UART on Kintex-7 FPGA," in *2020 12th International Conference on Computational Intelligence and Communication Networks (CICN)*, pp. 492–497, Bhimtal, India, 2020.

[25] M. Shabaz and U. Garg, "Shabaz–Urvashi link prediction (SULP): a novel approach to predict future friends in a social network," *Journal of Creative Communications*, vol. 16, no. 1, pp. 27–44, 2021.

[26] P. Jindal, A. Kaushik, and K. Kumar, "Design and implementation of advanced encryption standard algorithm on 7th series field programmable gate array," in *2020 7th International Conference on Smart Structures and Systems (ICSSS)*, pp. 1–3, Chennai, India, 2020.

[27] B. Pandey and R. Kumar, "Low voltage DCI based low power VLSI circuit implementation on FPGA," in *2013 IEEE Conference on Information & Communication Technologies*, pp. 128–131, Thuckalay, India, 2013.

[28] A. Kumar, B. Pandey, D. A. Hussain, M. A. Rahman, V. Jain, and A. Bahanasse, "Low voltage complementary metal oxide semiconductor based energy efficient UART design on Spartan-6 FPGA," in *2019 11th International Conference on Computational Intelligence and Communication Networks (CICN)*, pp. 84–87, Honolulu, HI, USA, 2019.