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Research Article

Indoor Art Display System under Computer Virtual Reality Visual Video Communication Transmission Signal

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This paper proposes a network video transmission system for indoor art display systems and visual video monitoring. Due to the problems of high mean square error, poor signal capture performance, and long timing jitter in current optical transmission signals, this paper proposes a low-rate narrowband IoT long-distance communication synchronization capture algorithm and optimizes the algorithm. The algorithm improves the visual center processing algorithm with high computational complexity into a simple look-up table calculation. This can simplify the calculation process and improve the system's operating speed. Finally, the paper implements a video communication indoor art display system with compatible multiple network interfaces based on high-speed multimedia DSP.

1. Introduction

Digital media art is a product of the modern information society. It is a combination of art theory and technology applied in digital media. It goes beyond the limits of two-dimensional planes from digital technology. Digital media gradually put all the facial features of the viewer into the virtual environment through computer language and image processing technology in interactive art and plastic art. Users can experience the peculiarities of art in a three-dimensional virtual space. The intervention of digital media art and the combination of display space combines space art and visual art. It is also the collision of three-dimensional space and two-dimensional space. It has become one of the focuses of people's attention that users conduct video communication on various existing networks. This paper briefly introduces a video communication system that conforms to the H.263 standard, is implemented based on high-speed multimedia DSP, and is compatible with multiple network interfaces. The system proposes a low-rate narrowband IoT long-distance communication synchronization acquisition algo-rithm [1]. The algorithm solves the problems of high error, poor captured signal performance, and long timing jitter. At the same time, this paper focuses on the core video processing part of the system. At the same time, this paper introduces the principle and composition of the interface part of PSTN, DDN, and IP networks.

2. System Introduction

2.1. System Structure. The overall structure block diagram of this system is shown in Figure 1. It consists of a core video coding module and three different network interface modules that can be flexibly chosen according to practical applications [2].

2.2. Video Codec. The video codec of this system adopts H.263 standard to realize in real time. The signal flow diagram is shown in Figure 2. The dashed box is the software implementation part of TM1300.

First, the video A/D digitizes the analog video signal from the camera and sends it to the video format conversion
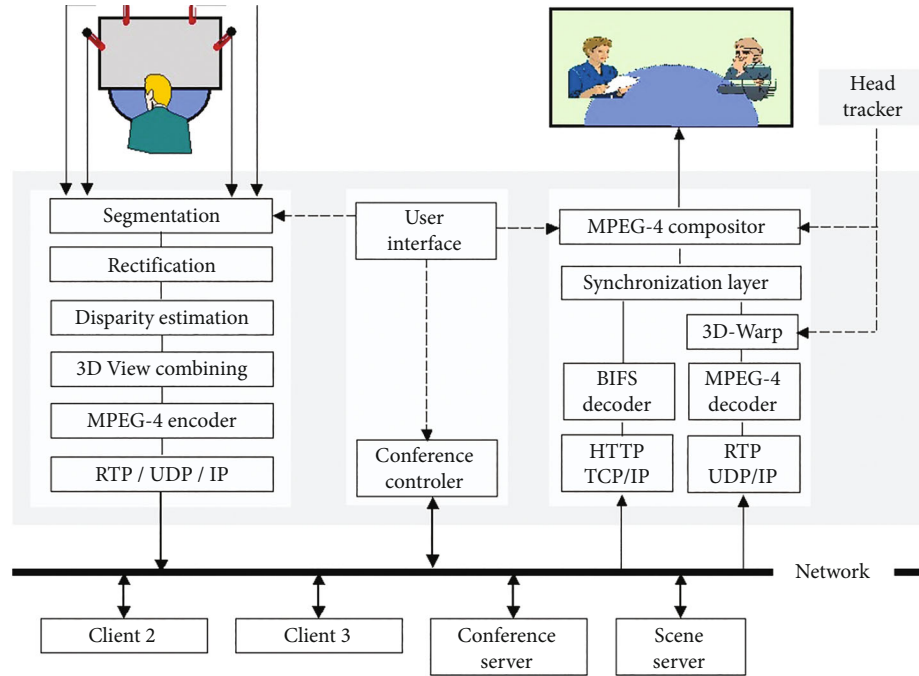
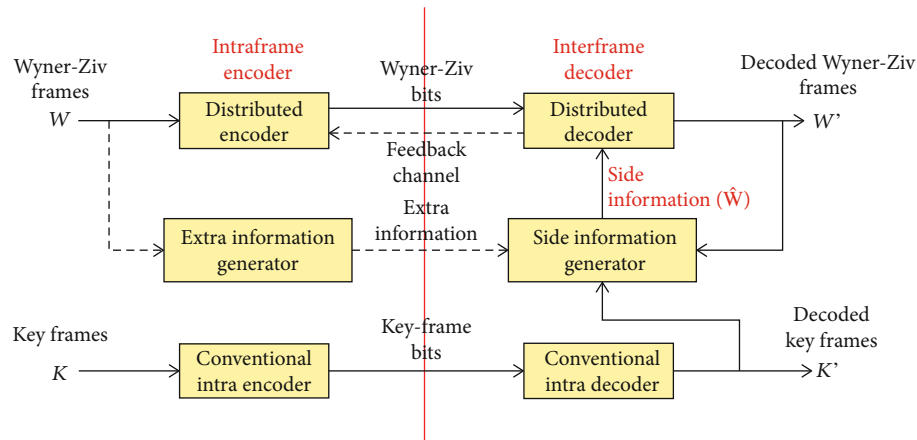FIGURE 1: Multi-interface video communication system structure.

FIGURE 2: Video codec flow chart.

part. In this way, we make the signal become CIF/QCIF data in YUV4: 2: 0 format required for H.263 encoding. Then, we put it into the relevant cache. The encoder then fetches the data from the buffer for encoding. The system puts the encoded data stream into the send buffer. The image data in the sending buffer is sent to the corresponding network through the communication interface unit through the SSI or PCI interface of the TM1300. The system then transmits the signal to the communicating party [3]. At the same time, the system also receives the data of the communication counterparty from the communication network and puts it into the receiving buffer. Then, the H.263 decoder extracts the data from the receive buffer, decodes it, and sends it to the display. In this way, the two communicating parties realize video communication through TM1300 and the communication interface unit.

3. Video Codec Based on TM1300

3.1. Software and Hardware Structure of TM1300. TM1300 is one of the TriMedia series products of high-performance multimedia DSP launched by Philips. It can process media information such as voice and video simultaneously on one chip. Its hardware module structure is shown in Figure 3.

Inside the TM1300 is an efficient VLIW core processor (DSP CPU). It is used to implement specific algorithms and coordinate and schedule all units on the chip. The processor runs under a real-time operating system and can provide interrupts and communication with other units on the chip. The CPU uses the VLIW instruction system [4]. The clock frequency is higher than 180 MHz. We can do five operations in parallel on one machine cycle. Each operation can contain several RISC operations. The TM1300 also
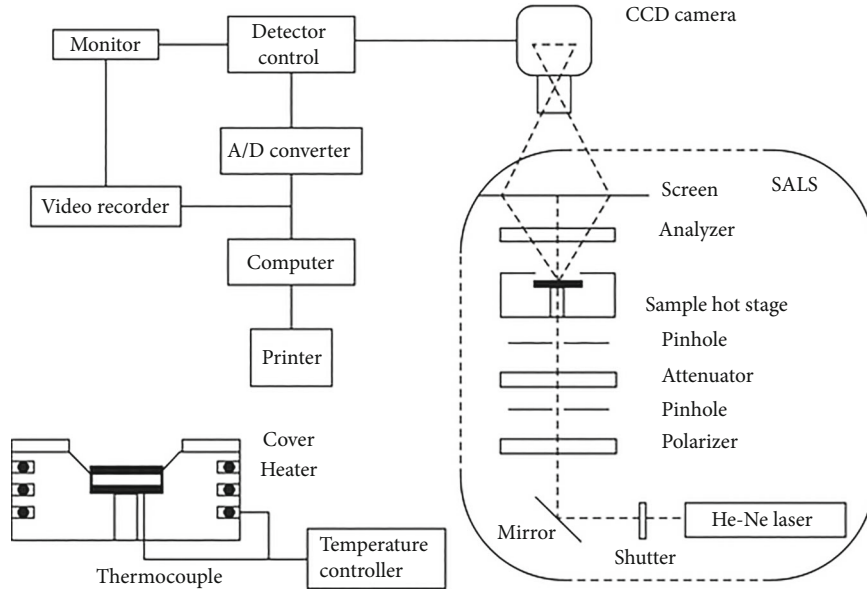
FIGURE 3: TM1300 module diagram.

contains a high-performance 32-bit bus, a memory system that is easy to store and access, 16 kB of data Caches, and 32 kB of instruction Caches.

TM1300 has an external I2C bus, PCI, and serial communication interface. The I2C bus interface facilitates the TM1300 to work independently from the computer. It has a maximum operating frequency of 33 MHz with a 32-bit PCI interface. This facilitates the connection between the TM1300 and the computer. Serial Synchronous Communication Interface (SSI) is a two-way channel for the TM1300 system to access the PSTN network or ISDN network.

The video I/O input unit of TM1300 can directly receive and output ITU-R656/601 standard YUV video data. According to the user's requirements, it can be set to a different capture mode or output mode. Audio I/O unit can directly receive and send serial digital voice data. TM1300 adopts an Image Coprocessor (ICP) and Variable Length Decoding (VLD) unit, which work independently in parallel with DSP CPU. The purpose is to reduce the burden of DSP CPU in image processing.

In the multi-interface system of independent models based on our multimedia DSP, TM1300 mainly undertakes tasks such as video/voice codec, code stream multiplexing, and communication control. The embedded real-time system pSOS manage the coordination between software modules. Set the driver function API, ecosystem, and user interface software and hardware relationship as Figure 4. A series of hardware of the development platform is the bottom layer of the system. It is managed uniformly by the pSOS real-time operating system. Based on the operating system, the driver functions of various hardware, such as the driver functions of audio and video codecs and the driver functions of input and output modules, are developed [5]. These functions can be called when developing application systems. The system's application software uses the services provided by the real-time operating system to complete based on these driving functions.
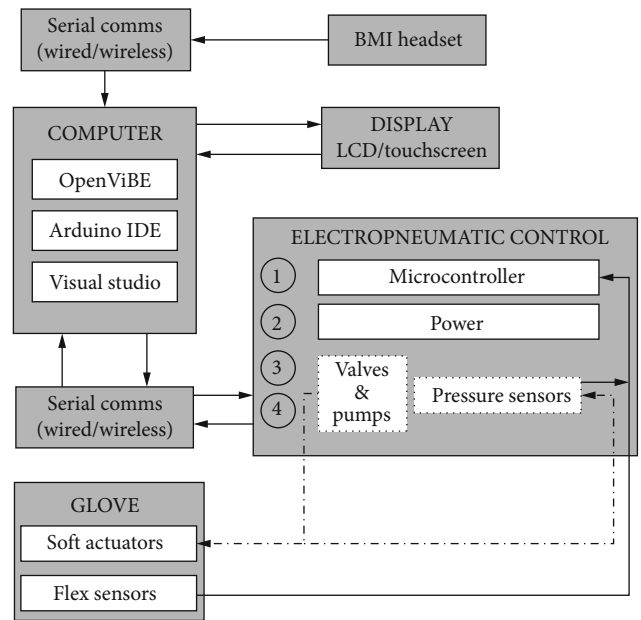

FIGURE 4: Schematic diagram of software and hardware relationship of TM1300.

3.2. Optimization of the Encoding Algorithm. We need to make the TM1300 work properly, but we also need to optimize the leading codec software. This is to ensure the real-time processing of the video signal. The optimization work of the software is considered from three aspects: the overall framework of the program, the specific algorithm, and the program code. This paper implements and optimizes the program in a layered manner, which conforms to the top-down, step-by-step refinement, and modular program design ideas. The layers are relatively independent [6]. The system can consider the different levels individually as needed. This is conducive to the transplantation and

redevelopment of the program. The global optimization in the overall framework layer can be determined by providing compilation parameters in the SDE of TM1300 or the integrated environment CodeWarrior. It is done automatically by the compiler. We can use grafting and global optimization techniques based on side information to improve program efficiency.

In the algorithm layer, optimization is mainly carried out for different algorithms. We use the self-developed New Prismatic Algorithm (NDA) for motion estimation, which is improved based on the New Three-Step Method (NTSS). It is assumed that the global minimum error point is monotonic in the neighbourhood of the search center. The number of search steps for NDA is indeterminate. It depends on the size of the search range and whether the minimum MAD point is at the center of the search. Of course, it is not excluded to make some code-level optimizations such as custom operations and matching algorithms for the motion estimation algorithm.

The code optimization of the code layer includes two methods: the automatic optimization of the program by the compiler and the manual optimization of the programmer. Due to the limitations of the compiler itself, manual optimization of the program before compilation is essential. In this paper, it is necessary to make full use of the five-time slots in each clock cycle when the DCT algorithm is optimized at the code level from the VLIW structure of TM1300. At the same time, we need to reduce unnecessary judgments and jumps and the number of decision trees. The system can also trade space for time by adding program code when necessary.

In terms of the communication signal model, this paper first establishes a low-rate narrowband IoT communication model:

$$S_{tr}(t) = \sum_{k=0}^{\infty} \sum_{k=0}^{N_f-1} w_{tr}\left(\begin{matrix} t - jT_f - kN_fT_f \\ -c_jT_c - t_{\text{start}} - b_k\Delta \end{matrix} \right). \tag{1}$$

w_{tr} represents a single pulse sent by the IoT. T_f represents the repetition time of the pulse. k stands for time-hopping sequence. c_j represents the additional time shift of the j pulse in the pulse train. T_c represents the unit additional time shift length. b_k denotes an extended stationary transmission symbol sequence. N_f represents the number of single pulses. Δ represents the modulation time shift. t_{start} represents the start time of signal transmission.

In the IoT communication model, the modulation time shift has a more significant impact on the model. We make improvements to the model as needed. The modulation time shift must meet the requirements of binary quadrature modulation. Also, set the start time $t_{\text{start}} = 0$ of the signal transmission [7]. At this time, the expression of the transmitted symbol in the signal model is as follows:

$$p_R(t) = \sum_{J=0}^{N_f-1} W_{tr}\left(t - c_jT_c - jT_f \right). \tag{2}$$

J represents the pulse width. This paper builds the channel model based on the tapped delay line. It is assumed that there are $L + 1$ taps in the model, and the channel state is quasi-static. The parameters in the model and the propagation delay are permanently fixed and set in the path delay. Let us call it $\tau_{l,0} = \tau_l - \tau_0$. In this paper, $\tau_{l,0} = \tau_l - \tau_0$ can be used to distinguish path delay and transmission delay. The signal received at this time is

$$S_{\text{rec}}(t) = \sum_{l=0}^{L} \alpha_l S_{tr}(t - \tau_l) = \sum_{l=0}^{L} \alpha_l \left(\sum_{k=0}^{\infty} p_T(t - b_k\Delta - kT_s - \tau_0 - \tau_{l,0}) \right). \tag{3}$$

α_l represents the low-rate narrowband signal factor. τ_l represents low-rate narrowband signal delay. Combining Equation (3), we simplify the $p_R(t)$ received symbol to the following expression:

$$\begin{cases} p_R(t) = \sum_{t=0}^{L} \alpha_1 p_T(t - \tau_{l,0}) = \sum_{j=0}^{N_f-1} h\left(t - c_jT_c - jT_f \right), \\ h(t) = \sum_{l=0}^{L} \alpha_l w_{tr}(t - \tau_{l,0}). \end{cases} \tag{4}$$

Then, the simplified signal model is

$$s_{rec}(t) = \sum_{k=0}^{\infty} p_R(t - b_k\Delta - kT_s - \tau_0). \tag{5}$$

Assuming that the time when the terminal receives the signal and synchronizes acquisition is t_{acq}, it is considered that the terminal starts to synchronize acquisition is after the signal arrives at the terminal and $t_{\text{acq}} > t_{\text{arrive}} = \tau_0 + t_{\text{start}}$ can be concluded. The synchronous capture time expression of the information is

$$t_{\text{syc}} = T_s \left\lfloor 1 + \frac{t_{\text{acq}} - t_{\text{arrive}}}{T_s} \right\rfloor + t_{\text{arrive}}. \tag{6}$$

T_s represents the average capture time. The punctuality of t_{syc} is the time when the signal arrives at the terminal. In this paper, it is assumed that the time when the signal arrives at the terminal is 0; then, the synchronous capture time expression of the information is simplified as

$$t_{\text{syc}} = T_s \left\lfloor 1 + \frac{t_{\text{acq}}}{T_s} \right\rfloor. \tag{7}$$

Based on the above signal model and the signal capture time expression, we identify the original signal and then calculate the communication synchronization acquisition algorithm.

3.3. Thread Synchronization and Priority Settings. In this paper, the mainframe of the program is constructed utilizing multithreading. This can meet the real-time requirements of
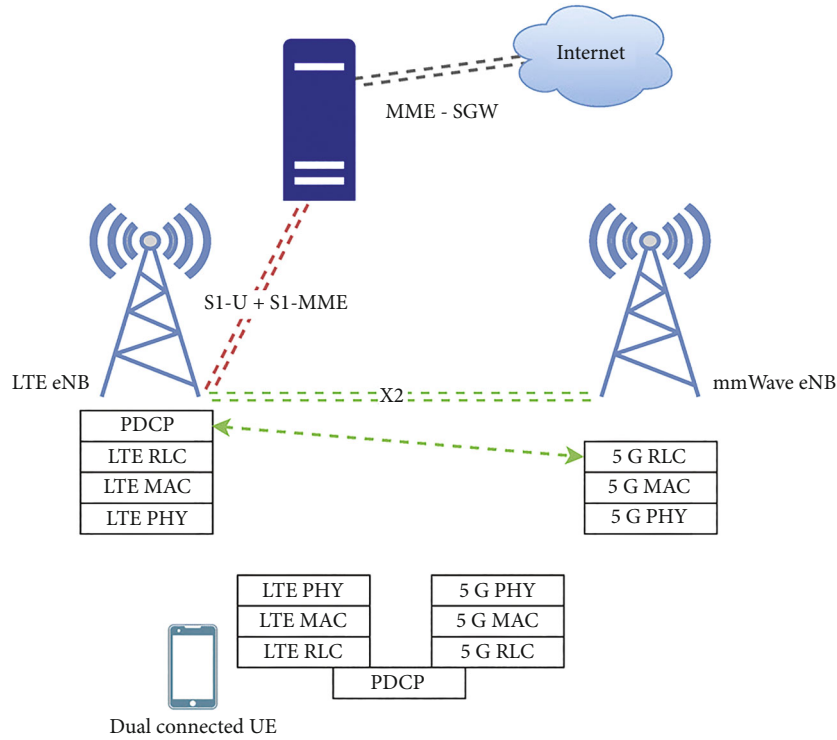
FIGURE 5: PSIN interface section.

video communication. There are four threads in the codec software implementation program: coding thread, sending thread, receiving thread, and decoding thread. Synchronization issues must be handled between them. Otherwise, the program will fail. We use critical sections and events to achieve synchronization between threads. For example, a critical section object can be used between the sending thread and the encoding thread to ensure that the reading and writing of the encoded data will not be performed simultaneously. This prevents deadlocks from being caused [8]. At the same time, the thread is synchronized through the event object to prevent the sending thread from not getting data from the sending buffer. At the same time, the algorithm can avoid the data overflow in the send buffer caused by the encoding thread. Similarly, we also use critical sections and events to synchronize the receiving thread and the decoding thread.

There is a specific limit to the network transfer rate. This dramatically affects the real-time performance of video communication. For this reason, we set the priority line according to factors such as different CPU time occupied by each thread and different degrees of threads being restricted by the outside world.

For example, we set the priority of threads that take up a long time on the CPU to a lower priority. We prioritize threads that use less CPU time to be higher. The decoding thread has a higher priority than the encoding thread, etc. This ensures that multiple threads work simultaneously and reduce the waiting time between threads. This method effectively increases the speed of video communication.

3.4. H.263 Encoding Control and Others. Since the interframe encoding function occupies the most CPU time in the H.263 encoding process, we must control it from a global perspective. This avoids a lot of unnecessary operations [9]. This article also makes full use of other coding techniques in the coding. Let us unpack some short loop statements. At the same time, we define appropriate function parameters to reduce the time spent in parameter passing. This avoids repeated pointer address operations to reduce the time it takes for the program to run.

4. Communication Interface

4.1. SSI Interface and PCI Interface. TM1300 provides an asynchronous serial communication port (SSI). Developers can design various communication interfaces by adding front-end chips (Figure 5). The SSI of TM1300 provides six interface lines to the outside world: receive and transmit data lines, receive clock and frame synchronization lines, and two flexible general-purpose I/O lines.

The primary function of the PCI interface is to make an interface between the TM1300 internal high-speed data bus and the external PCI bus. The purpose is to easily integrate the TM1300 system into the application system of the PC or in the embedded application system. TM1300 is the main CPU. We can supplement the functions that the TM1300 on-chip module does not have by plugging in other PCI devices—for example, our IP network interface board exchanges data with TM1300 through the PCI bus.
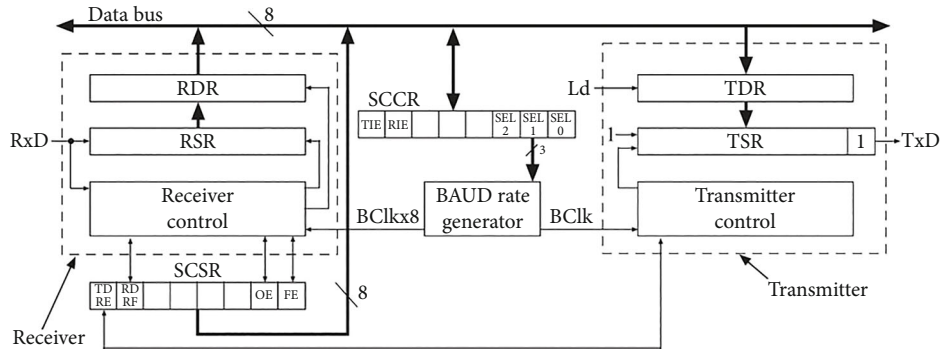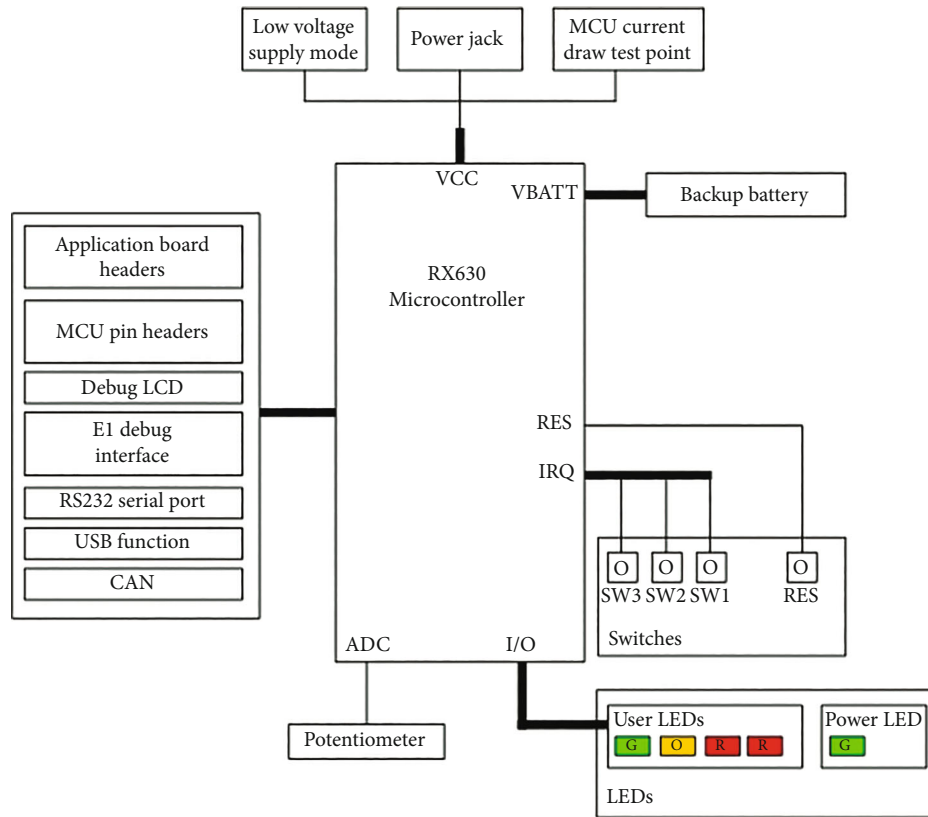
Figure 6: UART board block diagram.

Figure 7: E1 interface board block diagram.

4.2. UART Interface for PSTN. The communication unit for the PSTN network includes TM1300 and SSI, a general modem, and a UART interface board. The UART interface board sets up a communication bridge between the TM1300 and the telephone modem, as shown in Figure 5. The composition of the UART interface board is shown in Figure 6. Its function is to convert the data of the synchronous serial port of the TM1300 into the data format of the standard asynchronous serial port RS-232C, which is convenient to connect with the PSTN through the modem.

Among them, the programmable universal asynchronous transceiver (UART) is a FIFO with 16 bytes for the internal transceiver of ST16C550. It can realize serial-parallel and parallel-serial conversion of data. It provides

data and control signals to modems in the PSTN system and receives and records modem status information. The interface board's control and parameter setting functions are completed by a single chip 89C51.

4.3. E1 Interface for Digital Private Network. The E1 interface is the PCM introductory rate of ISDN. The rate is 2.048 Mbit/s. There are 32-time slots per frame. We call them TS0 to TS31, respectively. Each slot has an 8-bit code. It is equivalent to the transmission capacity of 64 kbit/s. Among the 32 time slots, TS0 is a frame synchronization time slot. TS16 is a signalling time slot. The role of the E1 interface board is to convert the synchronous serial port SSI of the TM1300 into a standard E1 interface. In this
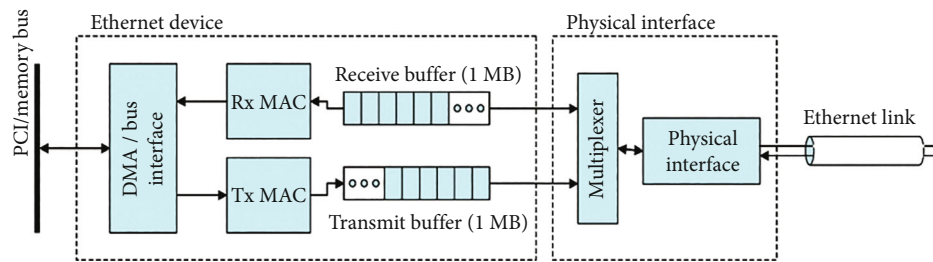
FIGURE 8: LAN interface board block diagram.

way, the communication function can be realized with the digital private network. The image data can also be placed in different time slots by setting the transmission rate as required. In this way, the rate of $n \times 64$ kbit/s can be formed.

The block diagram of the E1 interface board is shown in Figure 7. The critical chip is the E1 transceiver DS2153Q. It provides the essential functions required to connect to an E1 line. The chip's clock and data recovery circuit convert the HDB3 code received from the E1 line side into a nonreturn-to-zero code. We output the data to the buffer in the order of the time slots and then send it to the SSI port of the TM1300 via the buffer.

4.4. LAN Interface for IP Network. The block diagram of the LAN interface board is shown in Figure 8, and the key chip is RTL8029. The chip provides two main functions. (1) Provide a PCI bridge with TM1300. According to the PCI protocol, the system connects the sending and receiving data on the local area network with the PCI interface of the TM1300. This completes the interaction between RTL8029 chip data and TM1300. (2) Complete the data processing of the LAN interface link layer protocol. According to the link-layer protocol, the system unpacks the data from the local area network and sends it to the PCI interface part. At the same time, it packs the data from the PCI part according to the link layer protocol and then exchanges the level conversion part. The level conversion part completes the conversion task from the binary code to the signal waveform code suitable for transmitting the category 5 line of the local area network.

5. Conclusion

In this paper, a network video transmission system is proposed for the visual video monitoring of an indoor art display system. This paper proposes a low-rate narrowband IoT long-distance communication synchronization acquisition algorithm and optimizes the algorithm. The algorithm improves the visual center processing algorithm with high computational complexity into a simple look-up table calculation. Finally, the paper implements a video communication indoor art display system with compatible multiple network interfaces based on high-speed multimedia DSP. The experimental results show that our video communication system can complete essential video communication functions suitable for different networks. Digital media art is still moving forward as a developing subject. The exhibition space is still remarkably close to the people-oriented design concept. The practicability and integrity of the digital media artistic display space design in the era still need continuous exploration.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare no conflicts of interest.

References

[1] H. Wu and G. Li, "Visual communication design elements of Internet of Things based on cloud computing applied in graffiti art schema," *Soft Computing*, vol. 24, no. 11, pp. 8077–8086, 2020.

[2] F. Kujur and S. Singh, "Visual communication and consumer-brand relationship on social networking sites-uses & gratifications theory perspective," *Journal of Theoretical and Applied Electronic Commerce Research*, vol. 15, no. 1, pp. 0–47, 2020.

[3] B. Saris, "A review of engagement with creativity and creative design processes for visual communication design (VCD) learning in China," *International Journal of Art & Design Education*, vol. 39, no. 2, pp. 306–318, 2020.

[4] S. Jacques, A. Ouahabi, and T. Lequeu, "Remote knowledge acquisition and assessment during the COVID-19 pandemic," *International Journal of Engineering Pedagogy (iJEP)*, vol. 10, no. 6, pp. 120–138, 2020.

[5] K. Dooley, "A question of proximity: exploring a new screen grammar for 360-degree cinematic virtual reality," *Media Practice and Education*, vol. 21, no. 2, pp. 81–96, 2020.

[6] K. Lin, L. Wang, K. Luo, Y. Chen, Z. Liu, and M. T. Sun, "Cross-domain complementary learning using pose for multi-person part segmentation," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 31, no. 3, pp. 1066–1078, 2021.

[7] W. Andriyan and V. Anesti, "Visual audio communication design on the role of information technology on student life style of Universitas Raharja," *ADI Journal on Recent Innovation (AJRI)*, vol. 2, no. 1, pp. 194–203, 2020.

[8] G. Kaimal, K. Carroll-Haskins, M. Berberian, A. Dougherty, N. Carlton, and A. Ramakrishnan, "Virtual reality in art therapy: a pilot qualitative study of the novel medium and implications for practice," *Art Therapy*, vol. 37, no. 1, pp. 16–24, 2020.

[9] D. M. Hilty, K. Randhawa, M. M. Maheu et al., "A review of telepresence, virtual reality, and augmented reality applied to clinical care," *Journal of Technology in Behavioral Science*, vol. 5, no. 2, pp. 178–205, 2020.